Imperial College London / Faculty of Science and Engineering / Electrical and Electronic Engineering

FINAL YEAR PROJECT

"An Integrated Circuit Electrochemical Sensing Platform"

FINAL REPORT

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Abstract

Advances in medical science have been made possible by the increasing versatility, compactness and compatibility of semiconductor technology. This has enabled the miniaturization of implantable medical devices that help in the monitoring and detection of several important biomarkers. However, in order to make the existing medical technology completely harmless and benign to the user, much more research is needed in this field. This report gives insight into the development of a low power autonomous system that aims to minimise human intervention and configuration of implanted medical technology and alleviate issues of discomfort and stress caused from it. The report presents a minuscule readout circuit with an FSM based autonomous gain control unit and a $55\mu W$ 8 bit SAR ADC. The readout achieves an input dynamic range of 80dB along with a power consumption of $670\mu W$ and operates on a low supply voltage of $1.1V$. This report will explain the design of this technology and present the simulations and results obtained during its development. Information about background and relevant knowledge is also provided.

Acknowledgements

The work presented in this report was made possible by the help and effort of several other individuals. Firstly, my sincere thanks is towards the PHD students, Daryl Ma and Prateek Tripathi, who guided me throughout the course of the project and provided guidance in the development of various components. I would also like to thanks Professor Georgiou Pantelis who gave me the opportunity to take on this project under his supervision. Finally, I am also grateful for other technical and non-technical support from family and friends that kept encouraging me through the project.

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List of Abbreviations

List of useful Abbreviations:

IC	Integrated Circuit
DFF	D Flip Flop
ADC	Analogue to Digital Converter
DAC	Digital to Analogue Converter
AGC	Autonomous Gain Control
OpAmp	Operational Amplifier
OTA	Operational Transconductance Amplifier
TIA	TransImpedence Amplifier
NIA	Non-Inverting Amplifier
PGA	Programmable Gain Amplifier
VGA	Variable Gain Amplifier
FSM	Finite State Machine
SAR	Successive Approximation Register
CMOS	Complementary Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PMU	Power Management Unit
PWM	Pulse Width Modulation
VCO	Voltage Controlled Oscillator
WE	Working Electrode
RE	Reference Electrode
CE	Counter Electrode
LSB	Least Significant Bit
MSB	Most Significant Bit

1 Introduction

1.1 Overview

In the past few decades semiconductor technology has been developing rapidly. As silicon ICs continue to scale with Moore's law and become compact and low-powered, they become suitable for use in several different applications. One such application, that has arisen in recent years, is the field of personalised therapy.

Personalised therapy relates to the medicinal, therapeutic and curative treatment procedures that are accurately tailored to the need of the individual. Personalised therapy can be applied to the treatment of metabolic diseases such as Diabetes, Heart Disease, Obesity and others. This is because in several cases patients with these diseases have varying responses to external treatment, and so a more accurate and personalised means of treatment can go a long way in improving the health of such patients. Said treatment would rely on the the detection and monitoring of various metabolites through electrochemical sensing processes. By monitoring the concentration of endogenous metabolites we can track the activity and function of different physiological processes and by monitoring the concentrations of exogenous metabolites we can better understand the varying responses of each individual patient to the same pharmacological treatment [8].

Therefore, there is a growing need for developing a system capable of taking continuous measurements of target analytes. The information gathered from this can be used to construct an accurate understanding of the true needs of the individual patient and can help physicians prepare the most effective and least harmful response.

1.2 Objectives

The desired system should tackle the challenges involved in personalised therapy described in the previous section and be CMOS compatible to allow for creation of an ASIC. Such ASICs can be used with chemical sensing electrodes to employ several electrochemical sensing techniques to detect target analytes. These CMOS ICs can then be used to collect, process and transmit information about target analytes, which can then be used for various applications.

Such ICs collectively form a readout circuit. readout circuits are a crucial component of electrochemical sensing and this report, just like many others, aims to present the development of a unique readout circuit

The objective of this project is therefore to develop a robust low power, compact, and autonomous readout circuit that can be implanted into a host and will directly address several concerns when it comes to personalised therapy. For example, a continuous and real time measurement of glucose can made easier by automatic mode adjustments rather manual adjustments from an external source. More about the objectives of this project and problems addressed will discussed in later sections.

1.3 Report Overview

The report is structured into 11 sections as listed below along with a short description of the contents in each section:

- *Section 1, Introduction:* Provides an introduction to the project and briefly summarises the project objective and problems being addressed.
- *Section 2, Background:* Serves as the literature survey of the various concepts related to electrochemical sensing.
- *Section 3, Requirements Capture / Objectives:* Details the objectives of the project.
- *Section 4, Analysis Design:* A high level overview of the design is presented here along with comparisons from the interim report design proposal.
- *Section 5, Implementation:* A more in-depth overview of all the components of the readout developed and design strategies involved.
- *Section 6, Testing and Simulation:* The testing and simulations approach along with the results are illustrated in this section.
- *Section 7, Results discussion:* This section contains a discussion of the results.
- *Section 8, Evaluation:* A comparison of the final design with the objectives set out in Section 3.
- *Section 9, Future Work:* Further work and project improvements are detailed here.

- *Section 10, Appendix:* This contains information that can support the understanding of this report
- *Section 11, References:* The cited references throughout the report can be found listed here.

2 Background

2.1 Background Overview

The following section aims to provide the relevant information that is needed for the development of this project. Important electrochemical sensing techniques are explored and a survey of relevant literature is presented. This will provide background information of the several components that make up the full readout circuit and also give an understanding of other modules that are to be used together with the readout circuitry.

2.2 Electrochemical Sensing Techniques

Electrochemical sensing techniques are used to gather information on chemical compounds, such as the type or concentration of the chemical compounds. Some common techniques are described below:

- ***Potentiometry:*** Potentiometry is a technique used to find the concentration of a solute in a solution by measuring the voltage potential between two electrodes immersed in the solution [1].
- ***Amperometry:*** This technique allows you to find the concentration of an ion in a solution. It is done by imposing a fixed potential on a solution in the way shown in Figure 2.1. If this potential is the redox potential of the solution, then a current is generated that is proportional to the concentration of the solution. The current flows between the working electrode and counter electrode.

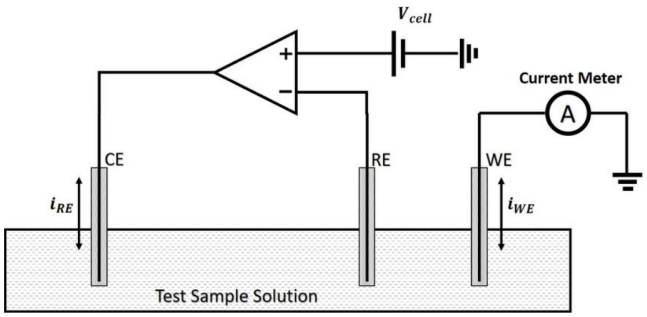

Figure 2.1: Simple Circuit use for Amperometry [41].

- ***Cyclic Voltammetry:*** This is another technique where a potential is swept in a linear ramp, in both the forward and reverse directions, between two switching potentials and the output current is measured.
- ***Square Wave Voltmeter:*** This technique can be used in lieu of Cyclic Voltametry. A symmetric square wave is superimposed on a staircase wave and the resulting wave is shown in Figure 2.2. This technique offers higher sensitivity and rejection to capacitive currents [34].

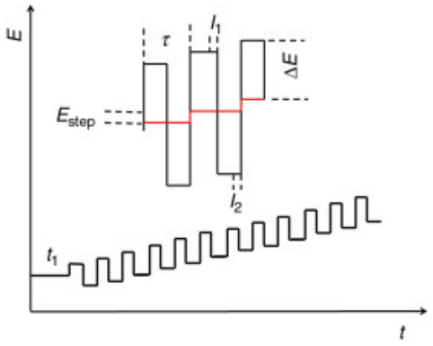

Figure 2.2: Square Wave Voltametry [16]

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Voltametry is often used to find the potential at which Amperometry needs to be done. In this project, the circuit developed is primarily to be used for amperometry. However, Cyclic Voltametry and Square Wave Voltametry are also possible approaches with the development of an appropriate potentiostat.

2.3 Electrode Configurations

The information that is received and processed by the readout circuitry is usually communicated in the form of a current. This current is generated by electrodes which are responsible for converting the chemical information in a solution into electrical information.

The standard electrochemical cell consists of three electrodes, the working electrode (WE), reference electrode (RE) and the counter electrode (CE). The working electrode is where the redox reaction occurs and a current is generated. The reference electrode is needed to apply a fixed cell potential across the RE and WE such that a redox reaction for the target analyte

can occur. It is therefore imperative that voltage potential at the RE is not allowed to fluctuate. This can be achieved by making the RE very large such that the resistance is low and the current flowing through it does not cause voltage variations, or by connecting the RE to a very high impedance so that no current flows through it at all. The former approach is not ideal as increasing the electrode size will make them too bulky to fit into a miniaturised system. The second approach will require the provision of a separate path for the current to flow and this is can be achieved by adding a counter electrode to the cell. Therefore the current in a standard electrochemical cell flows between the working electrode and the counter electrode. The electrochemical cell can be modelled as shown in Figure 2.3.

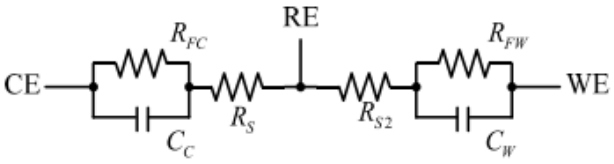

Figure 2.3: Electrode cell model [12].

In Figure 2.3 R_s and R_{s2} are the solutions resistances between the different electrodes. These are dependent on several factors such as concentration, type of ions and temperature. C_W and C_C are the double layer capacitances that exist between the electrode and cell interface. These capacitances can be are can be expressed in the following way:

$$C_W = A_{WE} \times K_{WE}, \quad C_C = A_{CE} \times K_{CE}$$

Where A_{CE} and A_{WE} are the areas of the CE and WE respectively and K_{CE} and K_{WE} are constants which relate to the material type of the electrode [3]. R_{FC} and R_{FW} are transfer resistances of the electrodes which are also related to the area of the electrodes. R_{FC} needs to be significantly lower than R_{FW} so that voltage applied using the RE appears across the RE and WE. Therefore the area of the CE must be significantly larger than the WE.

Figure 2.4 shows a 5-working electrode electrochemical cell configuration adopted from [14] and [15]. The 5 WEs can be seen next to the RE and a much larger CE. The electrodes for this project will be fabricated in this configuration.

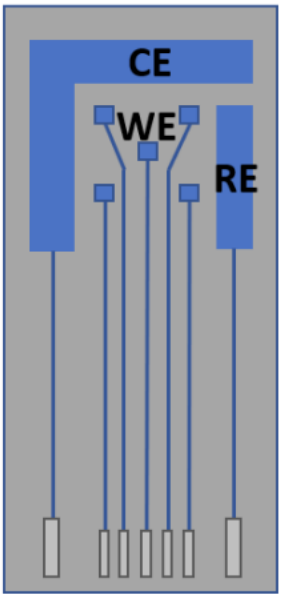

Figure 2.4: 5-Working Electrode configuration.

To increase the functionality of the electrodes, they can be coated with a substance that allows them to be more selective to the target analyte. Such substances can be oxidases which are used in the detection of various metabolites such as glucose, lactose, cholesterol and others. The term oxidase is used to refer to a large family of enzymes that catalyse a REDOX reactions involving oxygen molecules as the electron acceptor. Another class of enzymes known as cytochromes can also be used to coat working electrodes and increase their selectivity of several exogenous metabolites. Table 2.1 and Table 2.2 are taken from [14] and they show a list of oxidases and cytochromes that can be used to functionalise electrodes.

OXIDASE SPECIES	TARGET MOLECULE	DESCRIPTION	Applied Potential (vs AG/AgCl)
GLUCOSE OXIDASE	glucose	Metabolic compound as energy source	+550 mV
LACTOSE OXIDASE	lactate	Metabolic compound as marker of cell suffering	+650 mV
L-GLUTAMATE OXIDASE	glutamate	Excitatory neurotransmitter	+600 mV
CHOLESTROL OXIDASE	cholestrol	Metabolic compound that establishes proper membrane permeability	+700 mV

Table 2.1: List of oxidase enzymes

CYP SPECIES	TARGET DRUG	DESCRIPTION	Reduction Potential (vs AG/AgCl)
CYP1A2	clozapine	Antipsychotic used in the treatment of schizophrenia	-265 mV
CYP3A4	erythromicin indinavir	Used in the treatment of HIV and AIDS	-625 mV -750mV
CYP11A1	cholesterol	Metabolite able to establish proper cell membrane permeability and fluidity	-400 mV
CYP2B4	benzphetamine aminopyrine	Used in the treatment of obesity	-250 mV -400mV
CYP2B6	bupropion lidocaine	Antidepressant Anesthetic and antiarrhythmic	-450 mV
CYP2C9	torsemide diclofecan	Anti-inflammatory Diuretic	-19 mV -41mV
CYP2E1	p-nitrophenol	For the synthesis of paracetamol	-300 mV

Table 2.2: List of CYPs

2.4 Potentiostat Circuits

The potentiostat circuit is responsible for applying and maintaining the potential across a cell in the case of amperometric measurements or ramping the voltage upward or downward as is the case of cyclic voltammetry. A standard, single Op-Amp potentiostat circuit is illustrated in Figure 2.5.

The WE is biased at virtual ground and a cell potential equal to Vbias is applied by the OpAmp. Many variations of the potentiostat circuit have been used in previous works, with some attempting to solve certain problems. The potentiostat discussed in [30], for example, describes the operation of a fully differential potentiostat that has the capability for providing cell potentials that are twice the magnitude of what a single-ended potentiostat with the same supply voltage could provide. This allows the detection of many more analytes that have a cell potential which is too large for low voltage single-ended potentiostats. The problem with the circuit presented here is that the potentiostat uses two extra Op-Amps and so the power consumption and area usage is high.

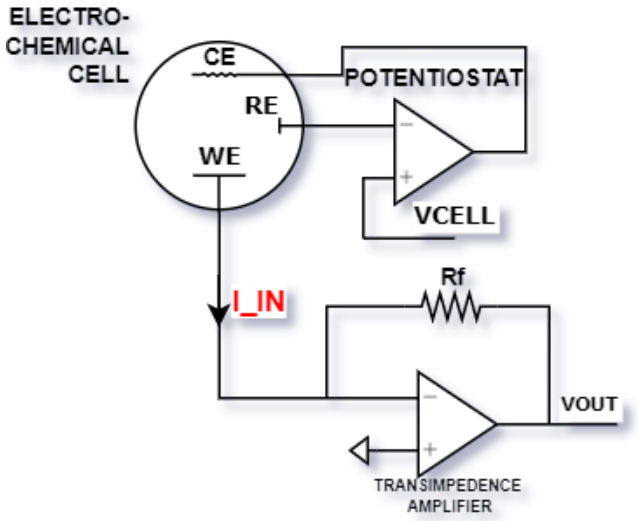

Figure 2.5: Simple potentiostat Circuit.

2.5 PMU

The power management unit is important as it generates the voltage rails for the all the active components. The circuitry can be wirelessly powered in the ways described in [4] and [31]. This will make the circuit more compact as there will be no large bulky batteries. Additionally, voltages below the supply voltage will also need to be generated for components, for example, reference voltages for the comparators need to be supplied. Techniques to generate constant offset voltages below the supply voltage are discussed [3]. The implementation of the PMU is not the purpose of this project and therefore it is not discussed in this report.

2.6 Important Considerations in view of previous work

These previous three components discussed, i.e. the electrodes, potentiostat and PMU, are all combined together with the readout circuitry to form an electrochemical sensing system. A high level block diagram of the full system can be seen in Figure 2.6.

2.6.1 Readout Overview

The main objective of this report is to develop the appropriate readout circuit for an electrochemical sensing system. Details about the desired qualities of such a circuit will be

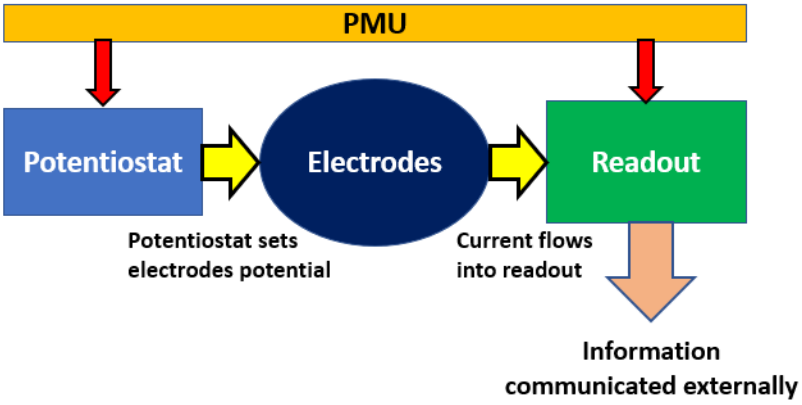

Figure 2.6: High level block Diagram of an electrochemical system.

discussed in Section 3. The readout circuit include all the components that take the input of the current coming in from the electrochemical cell, and convert, amplify and process it before passing it on to an external system. Most readout circuits generally contain at least an amplification stage and a digitisation stage. This is illustrated in Figure 2.7

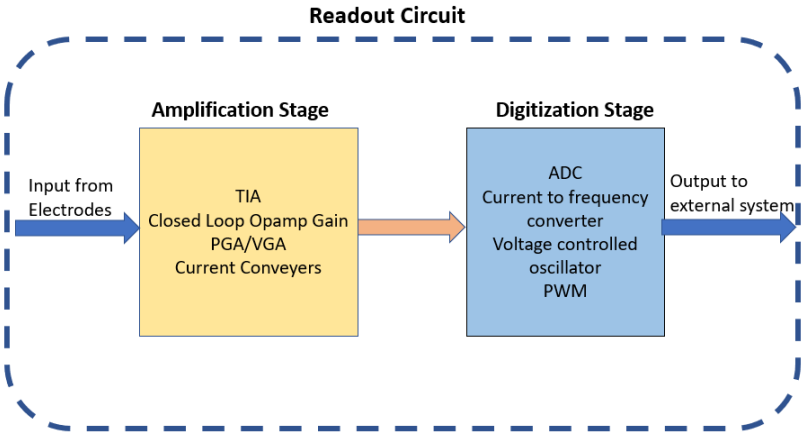

Figure 2.7: Readout Circuit.

The amplification and digitisation stage can be constructed in several different ways using components like those mentioned in Figure 2.7. Many authors from previous papers develop these components in unique ways to tackle concerns like size, power, and autonomy and versatility of circuits. More about the merits of these qualities and their relation to the project will be discussed in Section 3.

2.6.2 Amplification Stage

For the amplification stage, several attempts have been made to design a more compact readout. In [44], the authors attempt to make the circuit more compact by using the double-layer capacitance of the working electrode in the electrochemical cell as a circuit element and this saves area. In [27], the author attempts to share common resources used by different electrode arrays like a single gain stage among multiple arrays of electrodes. This sharing of resources allows the design to be a lot more compact. These attempts, however, are complex and are not necessary for the aims of this project. The sharing of components and the reduction in the number of active components [27, 44] also allows for lower power consumption. To achieve low power consumption, it is also important that the active components such as the OpAmps and OTAs must be optimised for lower power dissipation.

Previous works have also described various ways in which the circuits can be made more autonomous. A circuit with autonomy can be achieved by employing some kind of gain control. This allows the readout circuit to have a wide input range by responding dynamically to inputs of varying magnitudes. For example in [20], the authors use two comparators to determine whether an output voltage is within a certain desired range. If the voltage is out of range then, the gain control block adjusts the parameters of the switched capacitor integrator TIA. This changes the transimpedance gain and brings the output voltage back into the desired range. Another way is to use a separate programmable gain amplifier (PGA) in series with a TIA [12] to respond to inputs of varying magnitude.

2.6.3 Digitization Stage

Information is usually transmitted in the form of digital signals. Digital communication is less prone to noise and is more reliable. Therefore most readouts incorporate a digitisation stage, like the ones mentioned in Figure 2.7.

ADCs can be very useful in digitisation of the data with minimal loss of information but needs to be low-powered and compact. $\Sigma\Delta$ ADCs are often used as they can achieve a high resolution with a comparatively low power consumption. A $\Sigma\Delta$ ADC such as that discussed in [9] is a good contender for use in this project due to its $0.157mm^2$ compact structure and $241\mu W$ level power consumption. $\Sigma\Delta$ ADCs in [24] and [45] are also suitable in terms of power consumption and area.

Another kind of ADC, the capacitive SAR ADC was also studied as it also offered comparable power consumption. In addition to this Sigma-Deltas are slower than SAR ADCs and can exhibit cycle latency. As opposed to this, SAR ADCs have zero cycle latency, are very precise and easier to build. SAR ADCs can however suffer from lower maximum sampling rates [2]. A high level view of the full SAR ADC [10, 40] is shown in Figure 2.8.

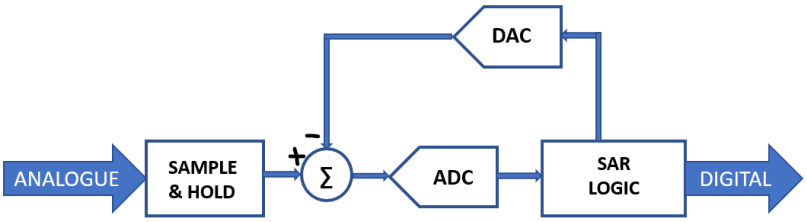

Figure 2.8: SAR ADC block diagram.

The SAR ADC uses successive approximation technique to convert an analogue input to digital output. Without any prior knowledge of the input voltage, a binary search algorithm is the most efficient algorithm and this can be incorporated in the SAR logic [40]. The SAR logic controls the DAC switches and the DAC output is subtracted from the sampled input. A comparator can then used to generate a digital output which depends on the polarity of the result of this subtraction. This comparator output is then used by the SAR logic to determine the next iteration. For an N bit conversion it therefore takes $N+1$ clock cycles (1 clock cycle for sampling the input and N for the binary search) to complete one full conversion cycle.

In this project a Capacitive SAR ADC will be used like the one shown in Figure 2.9, taken from [17]. Here, the sequence of capacitors implement both the DAC and the sample and hold circuit. V_{in} is sampled by the input during the sampling phase, after which switch s_B is connected to the supply voltage and S_A is opened. Switches S_0-S_4 are then controlled by the SAR logic accordingly.

The SAR logic can be designed using shift registers and code registers [6, 23]. Figure 2.10 shows two rows of DFFs implementing an 8 bit ADC. The top row forms the shift register which sets the code registers while the bottom row consists of the code registers that sets the output bits. When RST goes low a digital '1' is propagated rightwards from the top left DFF and this is used to force the output of the code register DFF high. Once the comparison is done, the COMP output is stored as the output bit of the code register DFF involved in the previous bit conversion when the next comparison cycle starts.

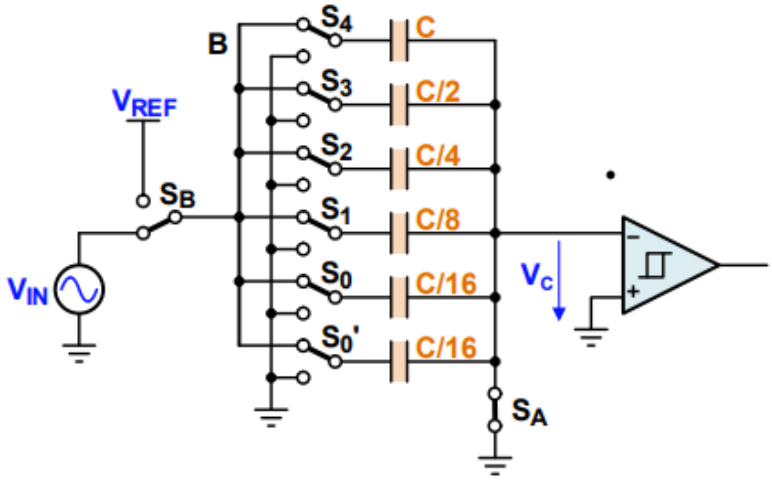

Figure 2.9: 5 bit Capacitive SAR ADC.

In another approach, instead of using the ADC, it is also possible to use a voltage to frequency converter such as that described in [11] to digitise the data. Here, the frequency of the output is dependant upon the voltage input. This has a higher power consumption of $1.03mW$ but offers a simpler structure and is still compact. PWM can also be used to digitise the data as done in [29]. Here the information is stored in duty cycle of the PWM signal.

2.7 Switches

Switches are an essential part of many readout circuits. The ideal switch does not exist and so CMOS based switches that are developed can cause several non-ideal effects. Common non-ideal effects in CMOS switches are as follows:

- R_{ON}**:** Single MOSFET switches have an on-resistance that is significantly dependent on the input voltage to the switch. To tackle this problem, Complementary switches should be used such as the ones shown in Figure 11.6.
- **Charge Injection:** This is usually the most significant issue when it comes to CMOS-based switches. When a CMOS-based switch opens or closes, the channel in the MOSFET needs to be removed or formed. When this happens, the switch injects an input dependent charge injection onto the connected capacitor plates. This is given by Q_{CH}

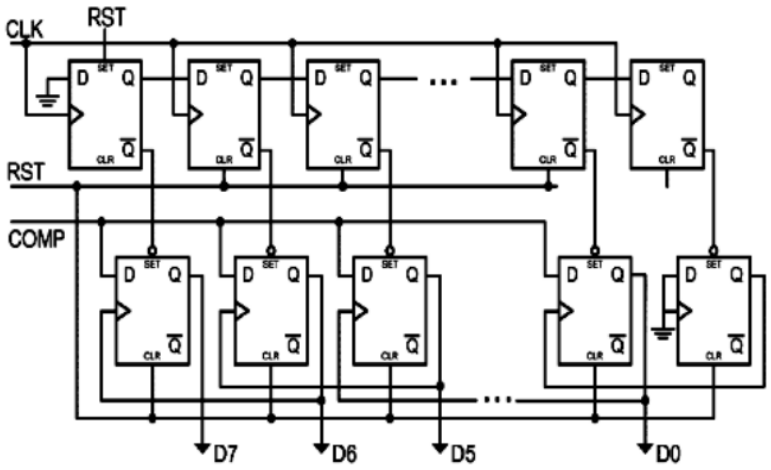

Figure 2.10: SAR logic implementation.

in the equation below [36]:

$$Q_{ch} = WLC_{ox}(V_{GS} - V_{TH}) = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

- **Clock Feed-through:** Clock Feedthrough is an error caused by capacitive coupling from the gate drain capacitor (C_{GD}) or gate source capacitor (C_{GS}) to the Hold Capacitor, (C_H) [43]. The Error caused by this is given by:

$$\Delta V = \frac{\Delta Q}{C_H}$$

- **Sampled Noise:** This is caused by the on-resistance of the switch which introduces thermal noise at the switch terminal that is stored on the hold capacitor C_H when the switch opens [35]. The noise is given by:

$$V_{noise} = \sqrt{\frac{kT}{C}}$$

- **Leakage:** In the case where the hold time for switches is very large, leakage currents through the switch can also lead to errors.

2.8 Comparators

Comparators were needed for the development of the autonomous gain control unit (see 5.5) and for the SAR ADC. Comparators are components that determine which of its inverting or non-inverting input has a higher positive value. If the inverting input of the comparator is higher, then then it outputs a 'digital-low' signal, and otherwise it outputs a 'digital-high' in the opposite case. A dynamic comparator is a comparator that is supplied a clock and only updates its output at the next clock edge. Such a comparator consumes less power as it is 'off' for half a clock period but needs to be clocked appropriately with the other clocked circuitry as it could lead to delays of one clock cycle and other timing issues. Two comparators with different topologies were developed and used for this project and these are discussed in Section 5.8.

2.9 Other Sources of information

A substantial amount of knowledge and information was also taken from several modules of Electrical Engineering, taught at Imperial College London. The module names are:

- Analogue Electronics 1, 2 & 3, (taught in year 1, 2, and 3 respectively)
- Digital Electronics 1 & 2 (Year 1 & 2)
- Biomedical Electronics (Year 3)
- Full Custom IC Design (Year 4)
- Analogue Signal Processing (Year 4)

This information includes biasing and sizing techniques, topology ideas and experience of Cadence software. Additionally, relevant information was also extracted from books like [5].

3 Requirements Capture / Objectives

The aim of this project is to develop an autonomous readout circuit for an implantable electrochemical sensing platform. This platform is intended to be able to use common electrochemical sensing techniques such as Cyclic Voltametry and Amperometry (discussed in Section 2) and continuously extract information about the concentration of the target analyte. In order to best suit the needs of the application, the platform is required to have the following characteristics:

- Autonomous: This is a central feature of the readout circuit which is aimed to set it apart from many other readout circuits. For systems that do not possess any degree of autonomy, frequent calibrations may have to be made to adjust some internal parameter. This may lead to an increased risk of irritation or injury to the host patient. Therefore it is imperative that the implanted system must have some degree of autonomy such that it can respond dynamically to different conditions and reduce the need for external intervention.

- Compact: In order for the electrochemical sensing platform to be used in biomedical applications for humans, it must be minimally invasive [19]. This is especially true for implantable devices as the platform is present inside the host at all times and smaller structures will be less noticeable and bothersome for the host. Therefore, it is imperative that the designed system is compact to cause minimal discomfort to the host.

- Low Power: The IC designed must be low power [7]. This satisfies two requirements. Firstly, high power dissipation means high heat dissipated into the surrounding tissue layers and this can cause thermal irritation and also tissue damage with prolonged exposure [25]. Low power devices will produce less heat, and so will be less harmful to the surrounding tissue layers. Secondly, it will be easier to wirelessly power the device, reducing the constraints on the power supply circuitry. The power consumption for the electrochemical sensing system was aimed to be less than $1mA$.

- Robustness and reliability: The host patients are at a great risk of injury if the implanted medical devices are damaged or faulty as this can cause severe pain and even death in some cases [22]. Therefore device reliability over a reasonable length of time is also extremely important.

- Bandwidth: The frequency of most biomedical signals ranges from a few Hz to several kHz [18]. This does not set a very stringent requirement on the bandwidth and most

circuit components should be able to operate in this frequency range.

- Diversified, selective and accurate: The platform may need to simultaneously detect the presence of different analytes. It also must be selective of the target analyte and provide accurate measurements of the concentration levels. The full system should be capable of doing this once the electrodes have been constructed out in the way described in Section 2.3. However, this is not a concern for the current project and is hoped to be investigated in future work.

The requirements laid out above are will be evaluated in Section 9 based on the actual implementation of the design.

4 Analysis of Design

The purpose of this section is to portray a high level design overview of the current system and compare this with the initially proposed system in the interim report.

4.1 High Level Design Overview

The full design for the readout circuitry with the amplification stage and digitisation stage clearly shown can be seen in Figure 4.1.

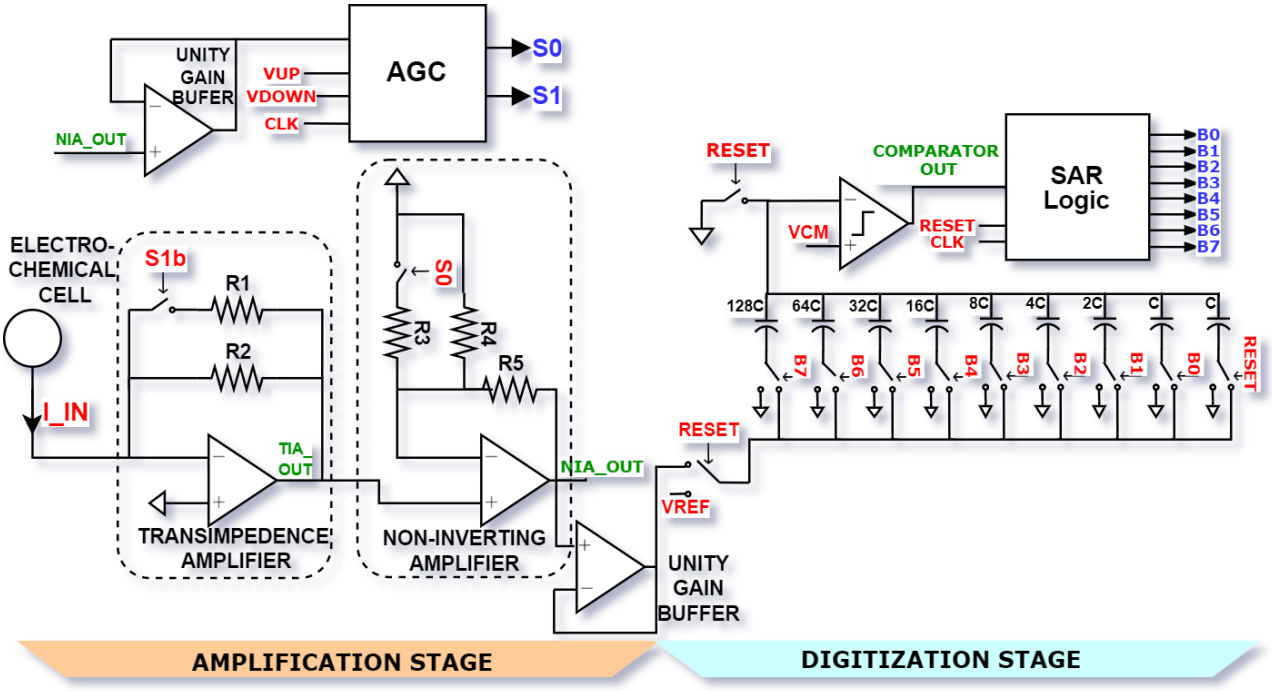

Figure 4.1: Complete high level view of readout design.

In the diagram above, the red text is used for signal being used as input to a device, blue text is used for outputs of the readout and green text is used for intermediate outputs. All 3-terminal switches shown connect to the top (right) branch when the control signal is a binary '1' and to the bottom (left) branch when the control signal is a binary '0'.

The input to the system is a current I_{IN} coming in from the redox reaction taking place in the electrochemical cell. This current is converted to a voltage by the transimpedence

amplifier (TIA) and the voltage is amplified by a non-inverting amplifier (NIA). *NIA_OUT* is then sent to the Autonomous Gain Control (AGC) circuit to check if the voltage is between V_{UP} and V_{DOWN} thresholds. When a threshold is breached, the AGC alters the gain of the TIA and/or the NIA using the switches shown in the diagram and this brings the voltage level back between the V_{UP} and V_{DOWN} thresholds.

NIA_OUT is also used as input to the Digitisation Stage of the readout, to convert the analogue voltage to digital before communicating it externally. The Digitisation Stage consists of a string of charge scaling binary weighted capacitors along with their respective switches that are used to sample the input when *RESET* is high and are also used as a DAC by the SAR ADC. The comparator provides input to the SAR logic block. Said block then uses this input to set the correct bits to represent the sampled input. At the end of the conversion phase bits $B0 - B7$ along with the gain setting $S0$ and $S1$ are communicated externally.

The two buffers after *NIA_OUT* are used to isolate the analogue circuitry from the digital circuitry. The prevents noise generated by the clock to feed-through to the analogue circuits. In this work, a simple unity gain low-power Operational Amplifier is used as the buffer. More detailed information about the operation of each individual component can be found in Section 5.

4.2 Comparison with proposed design

The proposed design for the complete electrochemical system at the start of the project is shown in Figure 4.2.

The basic operation of this design compared with the current design is the same, but a few changes were made over the course of the project. The features of the initially proposed design and the changes made are discussed below.

- *Supply:* A supply voltage of $1.8V$ to power all active circuit components is chosen. This is suitable for low voltage circuits and will be supplied by a power management unit (PMU). The supply voltage was later changed to $1.1V$ as this allowed for a lower power consumption. To assist in the biasing of transistors using this lower supply voltage, low V_{th} MOSFETs, as mentioned in Section 5.2 were utilised.

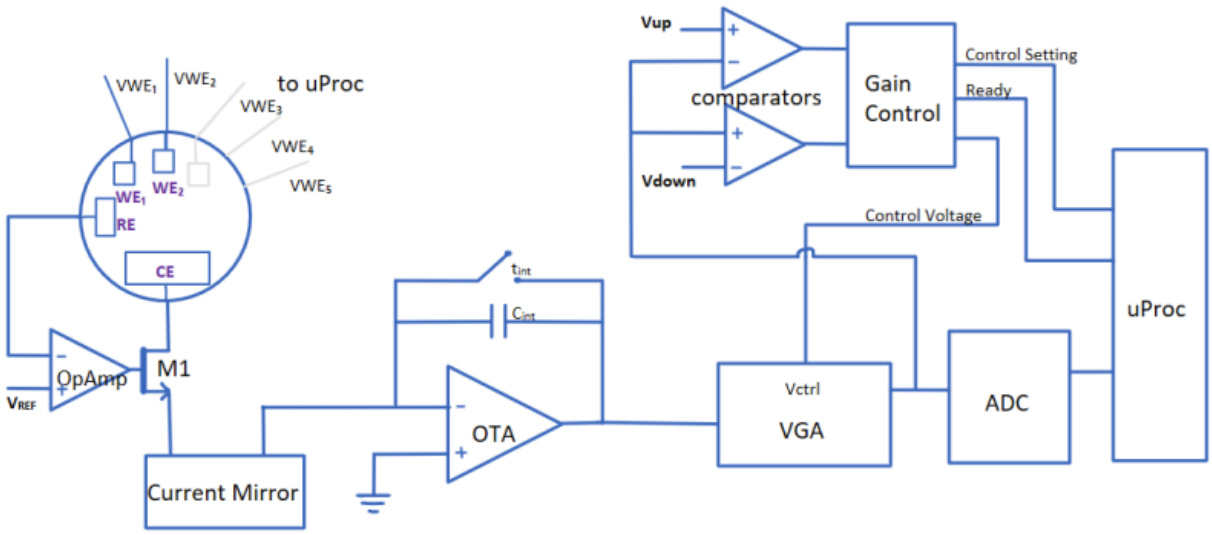

Figure 4.2: Proposed design at the start of the project.

- *Electrodes:* A representation of the electrochemical cell can be seen at the top left of Figure 4.2, with CE, RE and WE_x as the Counter Electrode, Reference Electrode and Working Electrodes respectively. The cell was previously designed to multiple working electrodes that are each specialised in the detection of one particular target analyte. In the circuit shown, each WE is biased at a different voltage so that the cell potential formed by each WE against the RE is the same as the reduction potential of the analyte targeted by the WE. Each WE was expected to also be coated with an enzyme to increase selectivity of the target analyte. Sufficient research was done to understand the operation of the five-working electrode configuration in the electrochemical cell and more information on this can be found in Section 2.3. Incorporating this into the project would have been a very demanding task and so given the time constraints it was deemed better to focus on the development of the readout circuit with autonomous gain control.

- *Potentiostat:* The potentiostat circuit is formed by the Op-Amp and the transistor M1. A constant reference potential V_REF is applied to the RE from the inverting input of the amplifier. The transistor M1 forms the feedback loop of the circuit, allowing the cell potential to be more stable in the presence of noise and variations. This circuit was expected to be developed alongside the Electrodes for the electrochemical cell. Therefore it was left out to focus on the main readout circuit.

- *Transimpedance Amplifier:* The OTA (Operational Transconductance Amplifier), C_{int} and the t_{int} switch form a switched capacitor transimpedance amplifier, where C_{int} is

the integration capacitor and t_{int} is the integration time. C_{int} and t_{int} define the output voltage of the TIA in the following way:

$$V_{out} = \frac{I_f * t_{int}}{C_{int}}$$

With I_f being the faradaic current coming from the REDOX reaction in the electrochemical cell. A switched capacitor TIA was used in the proposed design as it was thought to be able to save chip area as compared to a resistor. However, since the desired result was achieved without having to use a very large resistor, a resistive feedback TIA was used instead as discussed in Section 5.4. This also reduced the circuit complexity and allowed for easier calculations.

- *Gain Control and VGA:* In the proposed design in Figure 4.2, the AGC works in the same way as discussed in Section 5.5 but only controls the VGA to change the gain of the readout. The VGA that was planned to be incorporated in the design was based on the commonly known Gilbert cell topology. However, the total power consumption for this VGA was very high ($\sim 3mV$) and so it was abandoned and instead a PGA with two gain levels was used. Therefore, the AGC in the current design uses both the PGA and the TIA to alter the gain between four different gain modes as discussed in Section 5.5.

- *ADC and μProc:* The ADC is responsible for converting the analogue voltage signal into a digital signal and performs the same function in both proposed and current readout circuits. The design for the ADC architecture is explained in Section 2.6.3 .The output of the ADC and the gain setting are to be communicated to an external device such as a μProc which uses the reading to calculate the concentration of the analyte (the μProc design and coding is not the focus of this project).

5 Implementation

5.1 Implementation Overview

The section aims to convey a more detailed description of all the circuit components shown in the high level review in Section 4. All circuits were designed and simulated on Cadence Virtuoso using TSMC 180nm technology.

5.2 Active & Passive Components

All components were taken from the TSMC 180nm library. A *rnhpoly* resistor and *cfmom* capacitor was used where needed. In the case of MOSFETs, nch and pch devices which are standard V_{th} devices were used. In several instances low V_{th} devices were required for appropriate biasing in which case *nch_lvt_gb* was used for NMOS and *pch_lvt* was used for PMOS. These devices had a V_{th} that was generally several $100mV$ lower compared to the standard V_{th} devices.

5.3 Digital Sub-circuits

5.3.1 Logic Gates

Several gates needed to be appropriately designed for use in the digital components of the readout Chip. The gates designed were:

- Inverter
- 2-input AND
- 3-input AND
- 2-input OR

The widths of the PMOS and NMOS of these gates were adjusted such that the switching points could be as close to half of the supply voltage ($1.1V$) as possible.

5.3.2 DFF and DFF with asynchronous set and reset

A simple DFF was designed to be used in the FSM of the Gain control circuit. The structure of this DFF was taken from [13] and can be found in the Appendix in Figure 11.1.

For designing the SAR logic for the SAR ADC, a DFF with an asynchronous set and reset was designed. This was used for the implementation of the binary search algorithm, where the SAR logic needs to force high or 'set' each bit and compare it to the input voltage. The design for this DFF can be found in the Appendix in Figure 11.2 and was taken from [33].

5.4 Gain Stages

The OpAmps developed for both the TIA gain stage and the Non-Inverting Gain stage are both based on the two-stage simple differential cascode amplifier shown in Figure 5.1. Appropriate biasing was done so that all components were in saturation.

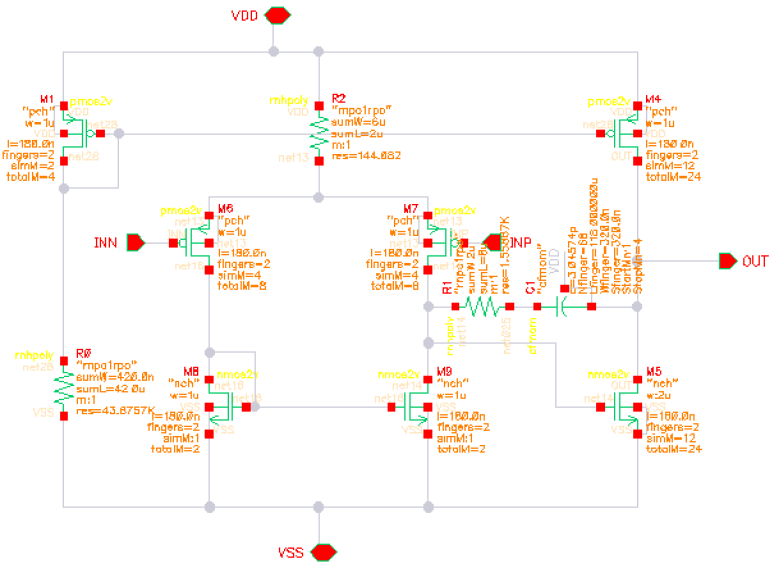

Figure 5.1: Simple Two stage differential amplifier topology used for TIA and NIA.

5.4.1 TIA

The TIA used in the readout circuit is shown in Figure 5.2. For an ideal TIA, the equation that relates the output voltage to the input current is given by:

$$V_{out} = I_{in} * R_G$$

where R_G is the Resistance in the feedback path of the TIA. This TIA has has two different trans-impedance gains, $656k\Omega$ and $23.4k\Omega$. It changes between in the two gain modes depending on the switch, which is controlled by the AGC. When the switch is closed, the $24.2k\Omega$ resistor is connected in parallel with the $656k\Omega$ resistor and so in effect the feedback path becomes a low resistance path. When the switch is open, only the $656k\Omega$ resistance is connected and so the feedback path becomes a high resistance path. Therefore in this way, the two approximate trans-impedance gains that can be achieved are:

$$G1_{TIA} = 23.4k\Omega, G2_{TIA} = 656k\Omega$$

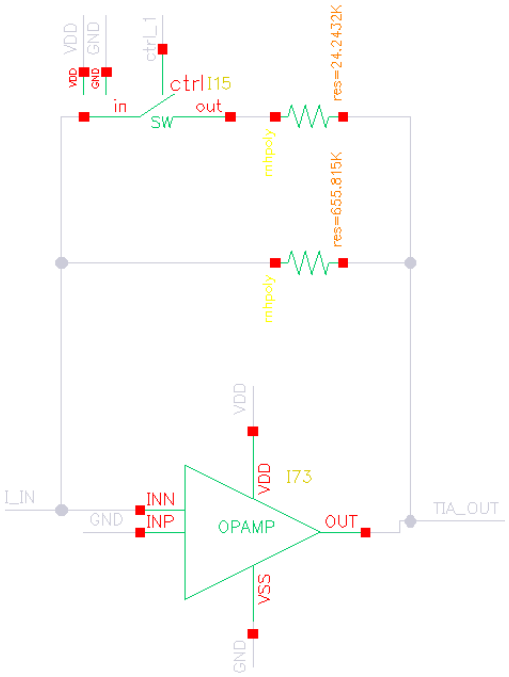

Figure 5.2: Transimpedence Amplifier.

5.4.2 Non inverting Gain OpAmp

The Non-inverting Amplifier (NIA) gain stage is shown in Figure 5.3. For the ideal case, the gain of a NIA is given by:

$$V_{out} = V_{in} * \frac{R_2}{R_1} + 1$$

The change of gain mode is done in a similar way to that of the TIA. The opening and closing of the switch in effect changes the 'R_1' value and hence the total gain. With 'R_2' being $60k\Omega$ and 'R_1' changing between $40k\Omega$ and 975Ω, the gain can be changed between the following two values approximately:

$$G1_{NIA} = 2.5, G2_{NIA} = 63.1$$

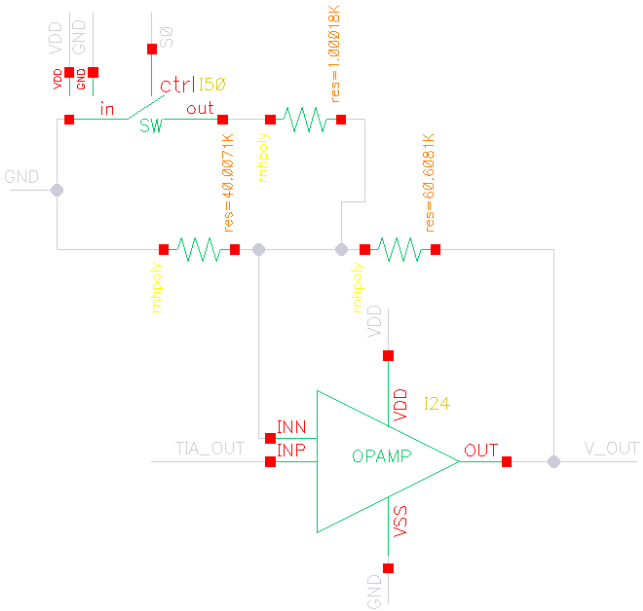

Figure 5.3: Non-Inverting Amplifier.

5.5 AGC

The AGC is responsible for adequately changing the gain mode of the readout in response to a wide range of input values. Figure 5.4 shows the structure of the full AGC. The two output bits from the AGC, Y0 and Y1, are used to control switches that alter the gain of the TIA and Non-inverting Amplifier Stage. There are four different modes and the AGC determines to switch between gain modes depending on the voltage level at the output of the second gain stage. This voltage is compared between two thresholds, V_{up} and V_{down} using two comparators. If the voltage crosses the V_{up} threshold, the output of the comparator goes 'high'. The comparator output is fed as an input into the FSM and this 'high' input signal indicates to the FSM to change its state and lower the gain. Similarly, when the voltage falls below the V_{down} threshold, the FSM is forced to change state and increase the gain. Therefore, the circuit is able to maintain the voltage at the output within a certain range, for a wide input range.

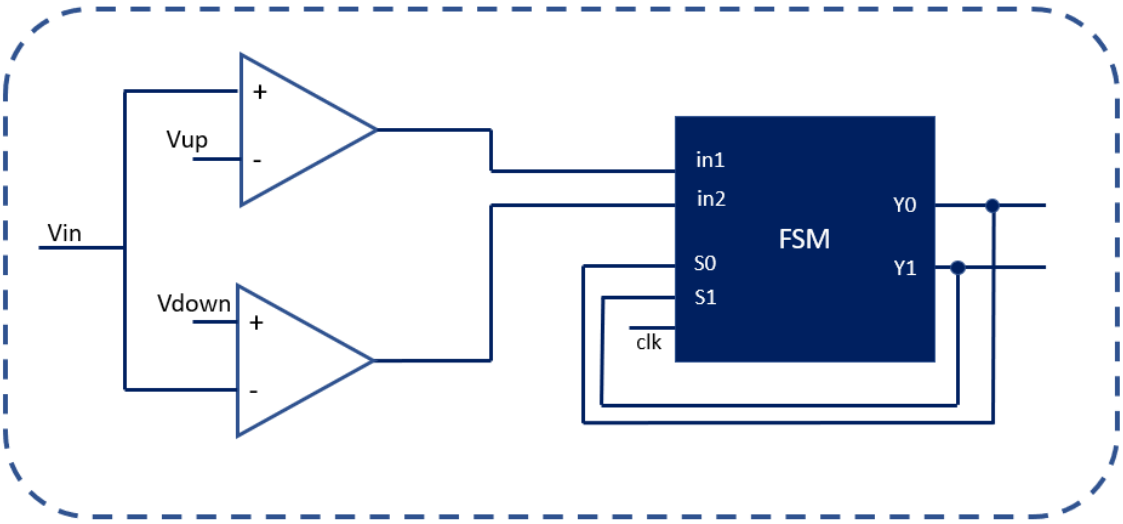

Figure 5.4: Autonomous Gain Control Circuit.

5.5.1 Custom FSM

The FSM is the most important part of the AGC. It has a set logic that determines the next state based on the input from the Amplifiers. The state diagram of the proposed FSM is as shown in Figure 5.5.

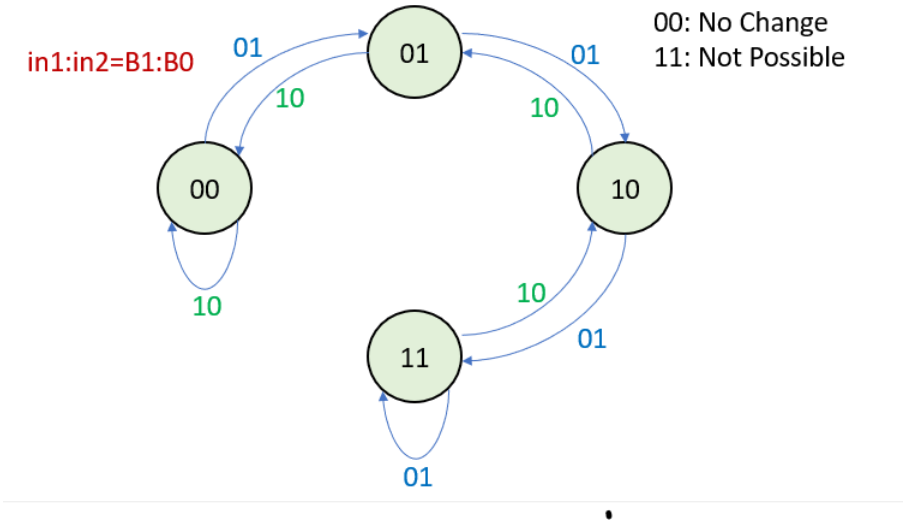

Figure 5.5: State Diagram for FSM.

It was also considered to use the following sequence:

$$00- > 01- > 11- > 10$$

to represent the increase increasing gain mode. This sequence will have a comparatively lower dynamic power consumption as it ensures that only one bit changes every time there is a state change. However, the disadvantage is that a separate output variable would have to be generated from the logic. In the case of the sequence used, the state variables and the output variables were the same and so there is no need to generate a separate output. Furthermore, the transitions are such that only twice does it happen that both state bits are changing, from $01- > 10$ and $10- > 01$. therefore it was appropriate to use the former sequence.

By then drawing out the state transition table and with the use of Karnaugh maps, the equations below were derived to give the next state of the FSM, based on current state and input. The state transition table and the Karnaugh maps can be found in the Appendix in Figures 11.3, 11.4 and 11.5.

$$S0^{+} = S1'.S2'.in2 + in1'.in2'.S0 + in1'.in2.S1 + S0'.S1.in1$$

$$S1^{+} = in2.S0 + in1'.S1 + S0.S1$$

From these equations the FSM was designed using the digital building blocks described in Section 5.3. This is shown in Figure 5.6 below. Edge-triggered DFFs are used to buffer the output bits S0 and S1 of the FSM, making sure they stay constant between rising edges of the clock signal.

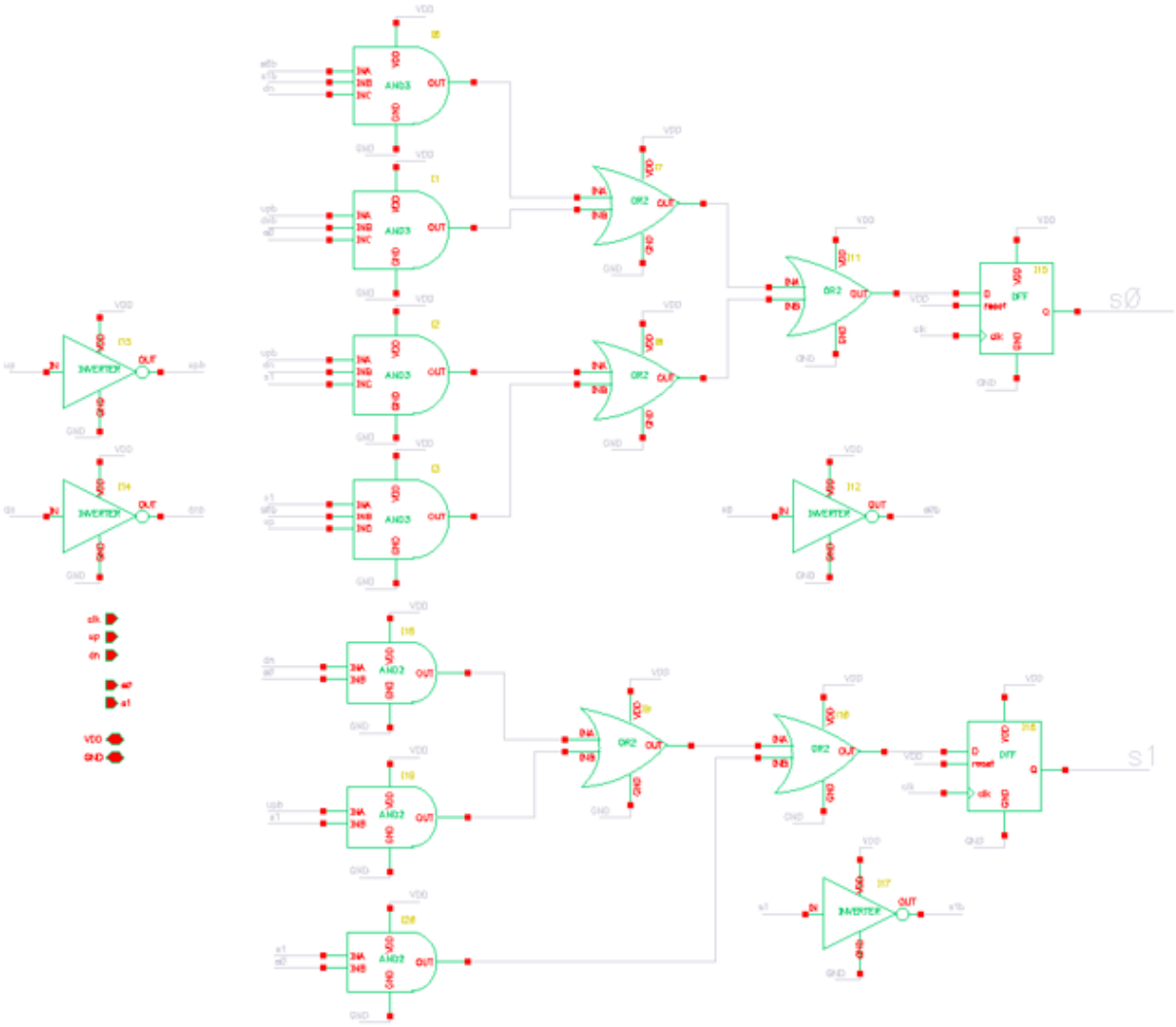

Figure 5.6: Schematic view FSM.

5.6 SAR ADC

The SAR ADC is responsible for converting the analogue input signal from the output of the amplification stage into an 8 bit digital signal. The topology chosen for the ADC was the SAR ADC, the operation of which is detailed in Section 2.6.3. The 5 bit capacitive SAR ADC shown in Figure 2.9 was extended to make an 8 bit capacitive SAR ADC. The full ADC schematic is shown in the Figure 5.7.

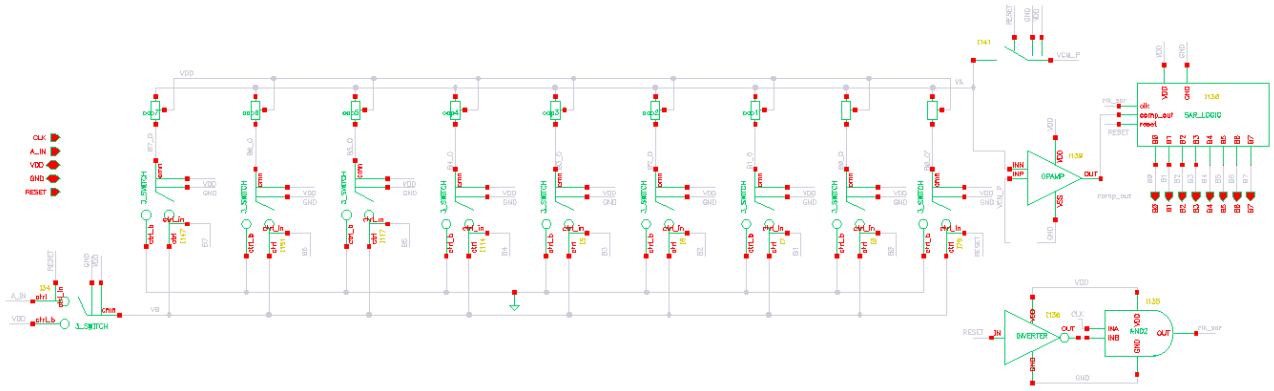

Figure 5.7: Schematic view of SAR ADC.

Figure 5.7 shows an array of binary weighted capacitors, with the LSB capacitor having a capacitance of $25fF$. The 3-terminal switches (see Section 5.9) connected to the bottom plates of the capacitors connect the capacitors to ground or to a voltage. This voltage is either the analogue voltage V_{IN} or V_{DD}, depending on whether the ADC is in sampling mode or conversion mode, respectively. The switches are controlled by the SAR logic module shown towards the right of Figure 5.7, and this module implements the binary search algorithm. The switch connected to the top of plate of all the capacitors is a bootstrap switch, discussed in Section 5.9. This switch connects the top plate of the capacitors to ground during sampling to the common mode voltage V_{CM} at the non-inverting input of the comparator. It was important to use the bootstrap switch here as the it minimises charge injection from the CMOS switch. Charge injection could add offset to the voltage at the inverting input of the comparator leading to an inaccurate conversion of the analogue signal.

An important difference between the implemented ADC and the one shown in Figure 5.7 is that the non-inverting input of the comparator is biased at V_{CM} $(550m)$ rather than ground [28]. This has several advantages as discussed in Section 7.2.

As this is an 8 bit ADC, it needs 9 clock cycles to complete one full analogue to digital conversion. The reset signal is a clocked signal that goes high every 9^{th} clock cycle and this is when the input voltage is sampled and bits B0 to B7 of the ADC are reset. As soon as reset goes low, the conversion phase starts in the next clock cycle and MSB bit (B7) is set high. Therefore the reset signal is enabled just before the next clock cycle, otherwise the reset would be registered as a high signal at this clock edge and the conversion would take one extra clock cycle. Therefore the combination of the inverter and AND gate shown at the bottom right of Figure 5.7 is to slightly delay the clock signal before passing it to the SAR LOGIC circuitry. This removes the extra clock cycle delay.

5.7 SAR logic

The SAR logic block was developed to implement the binary search operation and operate as discussed in Section 2.6.3. A few modifications to the design shown in Section 2.6.3 were made and these will be discussed in this Section. The full SAR logic block that was implemented for the SAR ADC can be viewed in Figure 5.8.

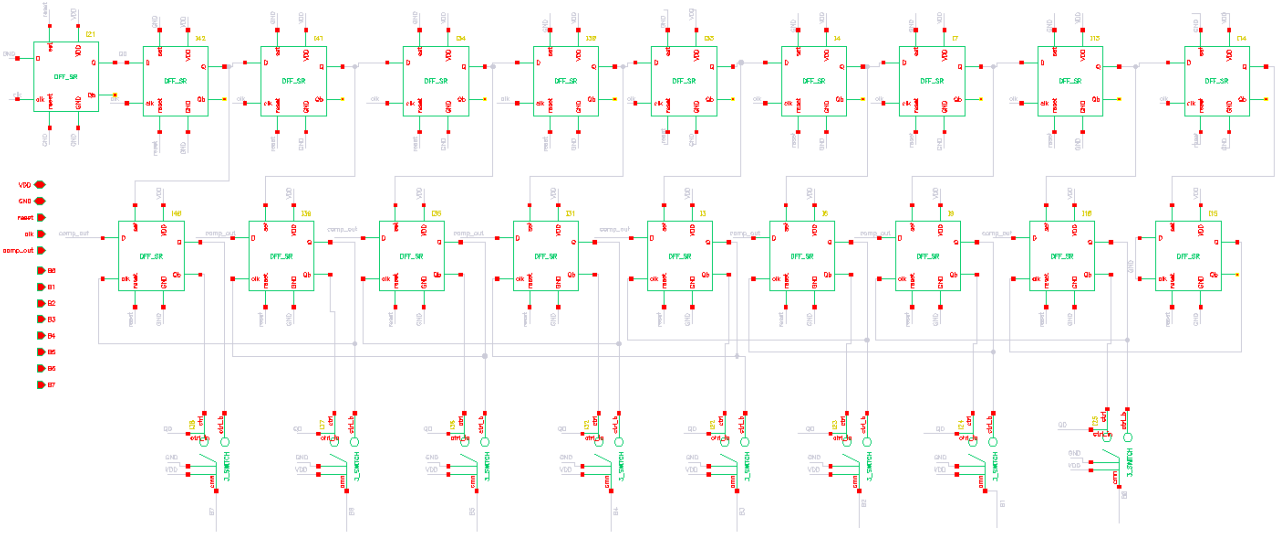

Figure 5.8: Schematic view SAR ADC logic.

The shift registers shown in Figure 5.8 are made from DFFs with asynchronous set and reset capability as shown in Section 5.3. An extra DFF is added to the left of the shift register DFFs to add an extra clock cycle for input sampling. The row of 3-terminal switches at the bottom of the Figure are controlled by RESET. In this way we can select between the two outputs Q and $\bar{Q}$ when RESET is off and on respectively. This is required as digital 'one' is needed by the DAC switches in the SAR ADC to connect to V_{IN} to sample it. When reset is high all the $\bar{Q}$ outputs of the code registers are high as well. As soon as RESET goes low, the regular Q outputs of the DFF are connected back and this stays true until RESET goes high again conversion phase.

5.8 Comparator Implementation

Two type of comparators were developed, one for use in the AGC and the other for the SAR ADC. The comparator that was used for the SAR ADC was made using differential cascode topology, show in Figure 5.9. The double cascode was added in order to increase the output resistance and hence the gain. This allowed the comparator to adequately detect small differences in voltage between its input and give the appropriate output accurately.

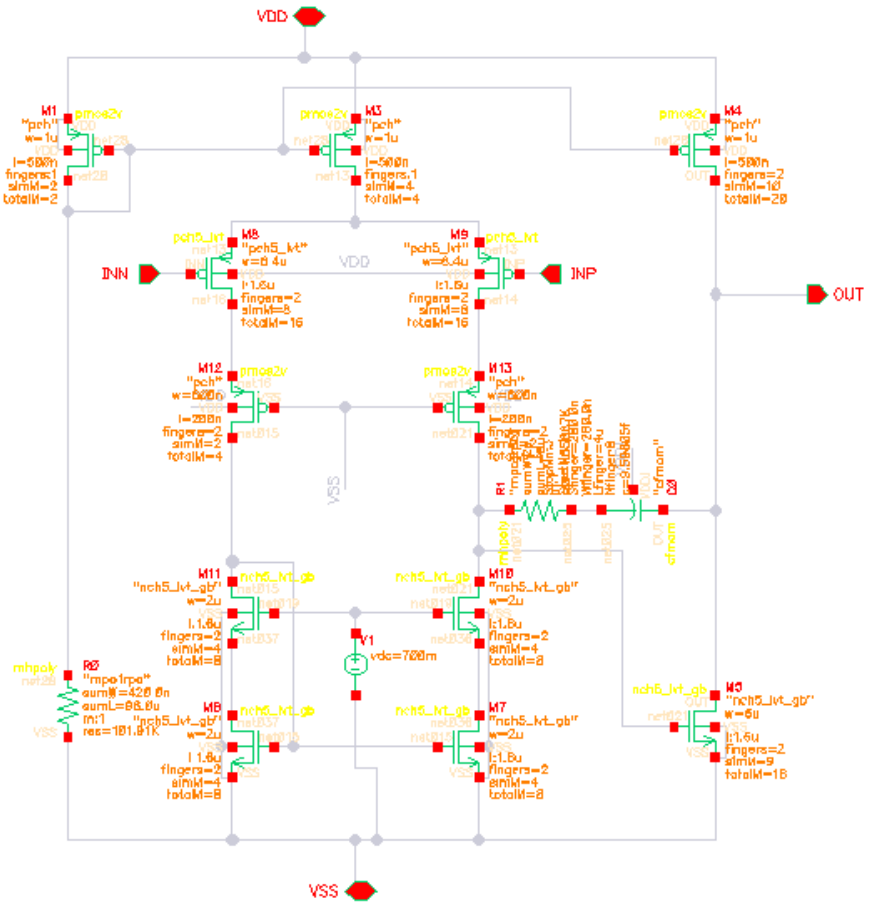

Figure 5.9: Double Cascode Amplifier used as a comparator.

A dynamic comparator used by the AGC, shown in Figure 5.10 was also developed as this consumed less power. They were used as the 'up' and 'down' comparators by the AGC. The one clock cycle delay caused by these comparators was mitigated by inverting the clock signal that was supplied to the FSM. Therefore, The FSM and the comparators in the AGC were using clocks that were 180 degrees apart. This meant that the 'latest' output produced by the dynamic comparators would be used by the FSM as required, rather the previous output

being used. This latency issue could not be removed in the SAR ADC and so the comparator in Figure 5.9 was used instead.

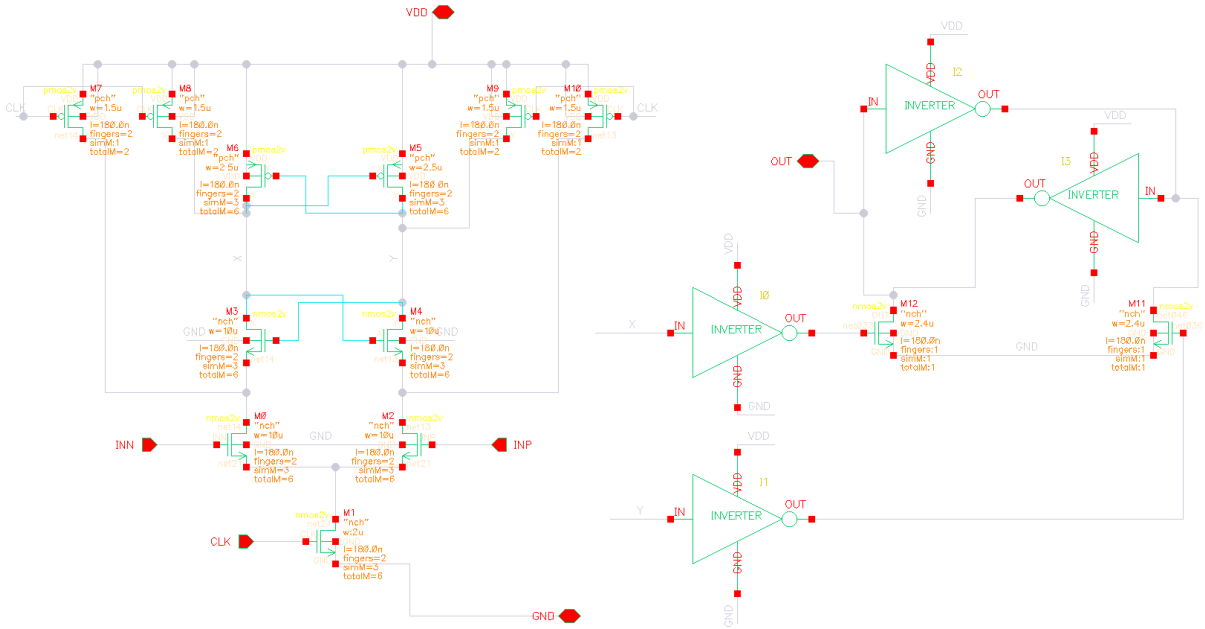

Figure 5.10: Dynamic Comparator.

Figure 5.10 shows a strong arm comparator followed by a SR-latch. The latch holds the voltages at the 'X' and 'Y' nodes steady while the clock signal oscillates. This circuit was adopted from [38] and [37] and its operation was verified for use in the AGC circuitry.

5.9 Switches

Analogue switches were designed for various parts of the readout circuit. Figure 11.6 was first developed and used by the gain control circuitry to alter the gain of the system. A complementary CMOS switch was used as this allows the on-resistance of a switch to be low and constant for a wide range of inputs. The extra inverter and delay module shown were added to make sure that the *clk* and *clk_b* clock signals are 180° out of phase. [35].

The switch was then extended using the same idea to make a 3-terminal switch and was used in several places in the SAR ADC. This switch is shown in 11.7.

Another switch, known as the bootstrap switch was also developed to further reduces the non-idealities. One major non-ideal effect with CMOS switches is that the MOSFETs introduce an input dependent charge injection on to a connected capacitor plate, when being turned on or off. This is shown in the equation below :

$$Q_{ch} = WLC_{ox}(V_{GS} - V_{TH}) = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

The bootstrap switch reduces this dependence by fixing VGS [36]. Boostrapping also allows the on-resistance of the switch to be more constant over a wide range of input voltage. The bootstrap switch developed is shown in Figure 5.11.

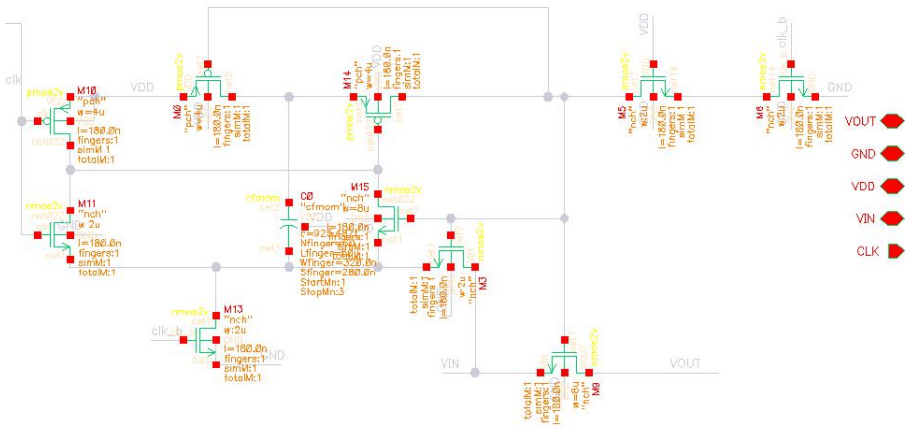

Figure 5.11: The bootstrap switch [42]

6 Testing and Simulation

All components of the readout circuit were simulated individually to make sure they operate in the desired manner. Three main analysis were run:

- **DC:** DC analysis was run for every transistor level component such as the OpAmps and comparator. DC operating points were used to make sure all transistors were biased appropriately and were operating in saturation. The DC analysis was then also used to observe the static power consumption of various components.
- **AC:** AC analysis was used for the TIA and NIA OpAmps. It was used to find out the gain, bandwidth and phase margin of the components. These are important parameters as they indicate the frequency range of operation and the stability of the component.
- **Transient:** Transient Analysis was implemented for several components to vary the dynamic mode of operation. This was crucial for the digital parts of the circuit such as the AGC and the ADC to confirm their real time behaviour. Transient analysis was also useful in analysing the slew rate of components like the comparator as well as its switching capability. This analysis was also needed to measure the real time power consumption of components over a sufficient period of time (eg. $1ms$), which was then averaged to find the average power consumption.

6.1 Switches

Switches were tested to assess their switching capability. A transient analysis for the bootstrap switch is presented in Figure 6.1 and the schematic for this can be found in the Appendix in Figure 11.8.

Figure 6.1 shows that switch is able to switch between an input voltage of $800mV$ and ground for an input frequency of $500kHz$ and clock edge rise and fall times of $1ns$ each. A similar analysis was run for the 2-terminal and 3-terminal switches as well.

Table 6.1 presents the power consumption of the switches. The switches consumed a much more significant amount of power when they were closed as compared to open. Hence, the average worst case power consumed by the three types of switches was found for the case that they are always on and result can be found in Table 6.1.

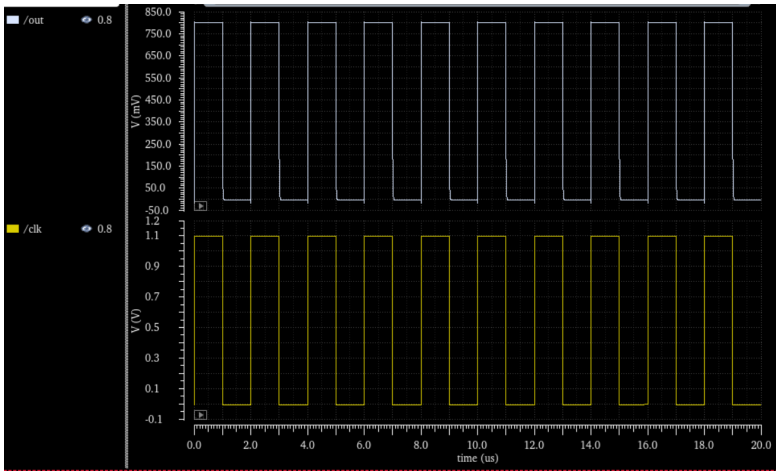

Figure 6.1: The bootstrap switch switching between $800mV$ and ground

Switch Type	Power Consumption (nW)
Boostrap	**81.75**
3-Terminal Complementary	**17.61**
2-Terminal Complementary	**15.14**

Table 6.1: Power consumption for each switch type.

From Table 6.1 it is observed that the bootstrap switch has a significantly larger power consumption compared to the other two switches. In addition to this, the bootstrap switch also has comparatively a very large area coverage, particularly due to the 1pF capacitor being used (see Figure 5.11). It is for this reason that the bootstrap switch is only used in one location, (see Section 5.6) despite having a superior performance in terms of its charge injection and on-resistance.

6.2 Comparators

This section contains the simulation results for the two comparator topologies that were discussed in Section 5.8.

Figure 6.2 shows the transient analysis of the comparator when switched between ground and V_{DD}. Figure 6.3 shows a high gain for the double cascode amplifier of $100.8dB$ with a unity gain frequency of $64.79MHz$. The phase margin was not a concern for the comparator as it is to be operated in open-loop.

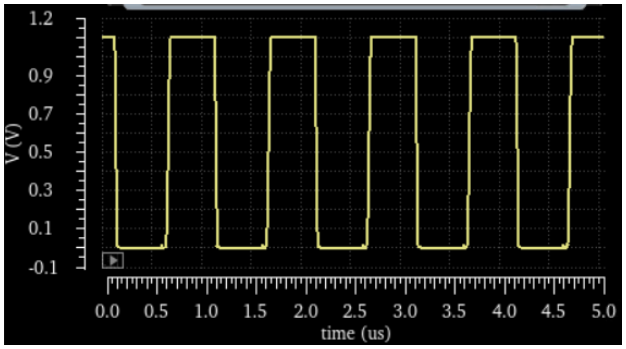

Figure 6.2: Transient Analysis of double cascode comparator.

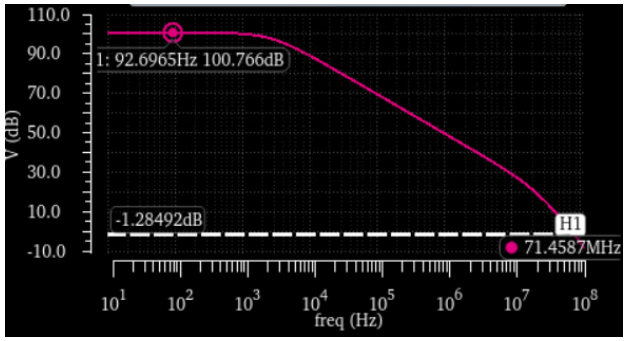

Figure 6.3: AC analysis of double cascode comparator.

Figure 6.4 shows the transient simulation of the dynamic comparator. The OUT signal switches between V_{DD} and ground depending on whether v_{inp} or v_{inn} is higher. Signal X is the output node of the strong arm comparator while the OUT signal is taken from the output of the SR-latch (see Figure 5.10), and is held constant by the SR latch while the clock is switching.

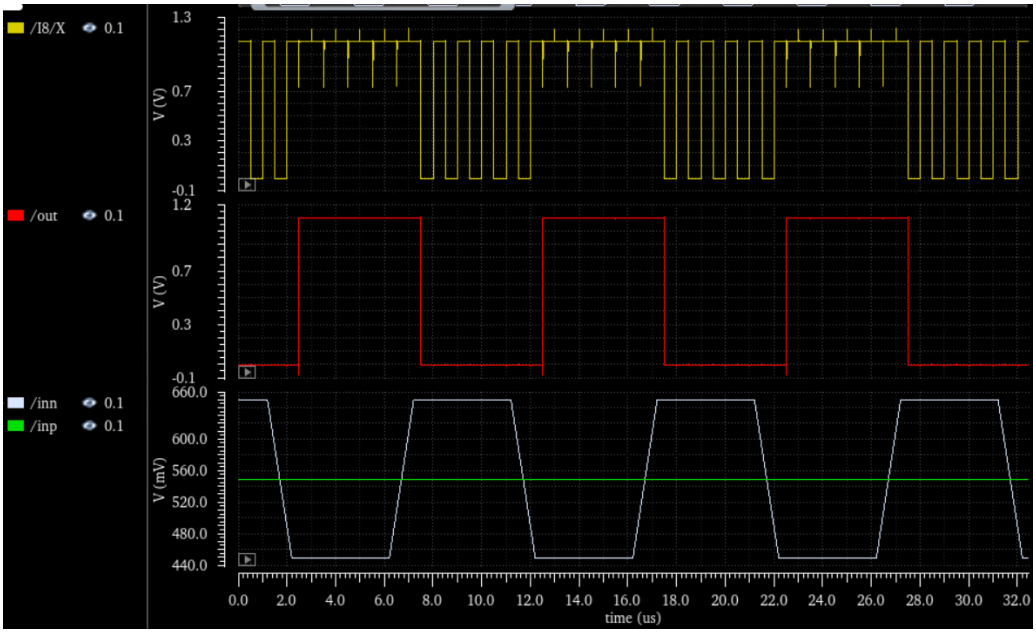

Figure 6.4: Transient analysis dynamic comparator.

The average power consumption for a 50% high and 50% low output was then also measured for both comparators and this is summarised in Table 6.2. The Dynamic Comparator is seen to have a much lower power consumption. This is because it only consumes power in the presence of a clock and is then turned off.

Comparator	***Average Power consumption*** μW
Dynamic Comparator	1.30
Cascode Comparator	39.0

Table 6.2: Power consumption for each Comparator type.

6.3 AGC

6.3.1 FSM operation

A transient analysis was run to verify that the 'Up' and 'Down' comparators triggered appropriately and that FSM logic was working appropriately. The results of the transient analysis can be found displayed in Figure 6.5. More information about the FSM operation can be found in Section 5.5.

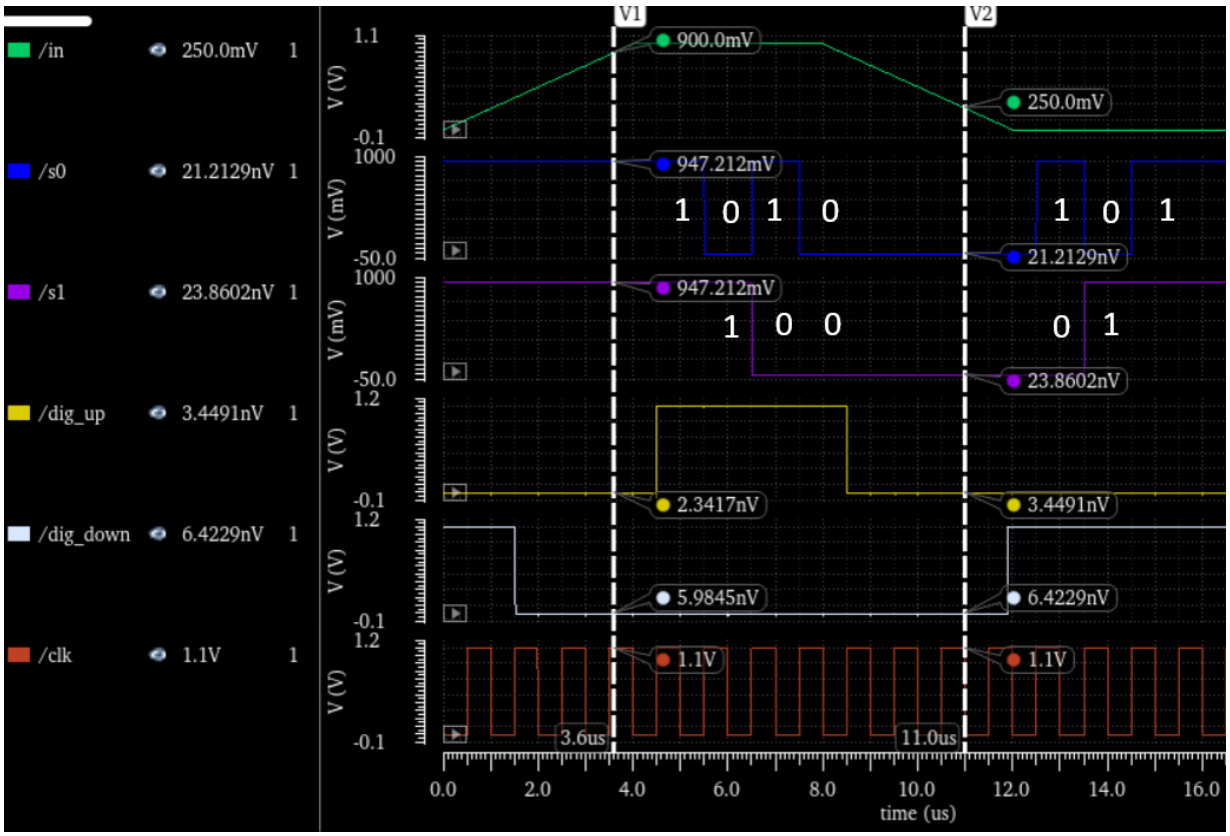

Figure 6.5: Transient analysis of AGC and FSM.

An artificial input voltage is swept from $0V$ to $1V$, held constant for $4\mu s$ and then swept back down. The threshold voltage for the upper comparator and lower comparator is set to $900mV$ and $250mV$ respectively, with *dig_up* and *dig_down* being the respective comparator outputs. The dynamic comparators are clocked with a 1MHz clock, also shown in the Figure 6.5. As the input voltage passes the $900mV$ threshold, the output of the upper comparator is seen to go high on the next clock edge and the lower comparator works in the same way as well. S1:S0 are the state bits of the FSM, which are also the output of the FSM and AGC.

When *dig_up* is high, the state bits change from:

$$11- > 10- > 01- > 00$$

This is representative of a reduction in gain intended to bring the voltage level down at the output of the gain stages. Likewise when *dig_down* is high the stage bits change in the manner:

$$00- > 01- > 11- > 10$$

This represents an increase in gain by 4 modes increasing the voltage level at the output of the gain stages.

When *dig_up* or *dig_down* are constantly high, the state bits cannot change due to the input current to the readout circuit being either too high or too low, and so the gain of the system is either at its minimum or at its maximum.

6.3.2 AGC power consumption

The comparators and FSM circuit were the components that were dissipating power in the AGC. The power consumption of the AGC was calculated by simulating the AGC over $20\mu s$ and sweeping the input voltage up and down. The combined current going through VDD for all these components was plotted and the instantaneous power was calculated by multiplying it by the supply voltage ($V_{DD} = 1.1$). The resulting graphs is plotted in Figure 6.6.

State Bit	Power
11	$209.7\mu W$
10	$106.3\mu W$
01	$105.9\mu W$
00	$6.32\mu W$
Average	$107.1\mu W$

Table 6.3: Power consumed in each FSM State

From the graph it can be seen that the power consumption is significantly dependent on the state of the FSM. The average power consumption for each FSM state was found and is

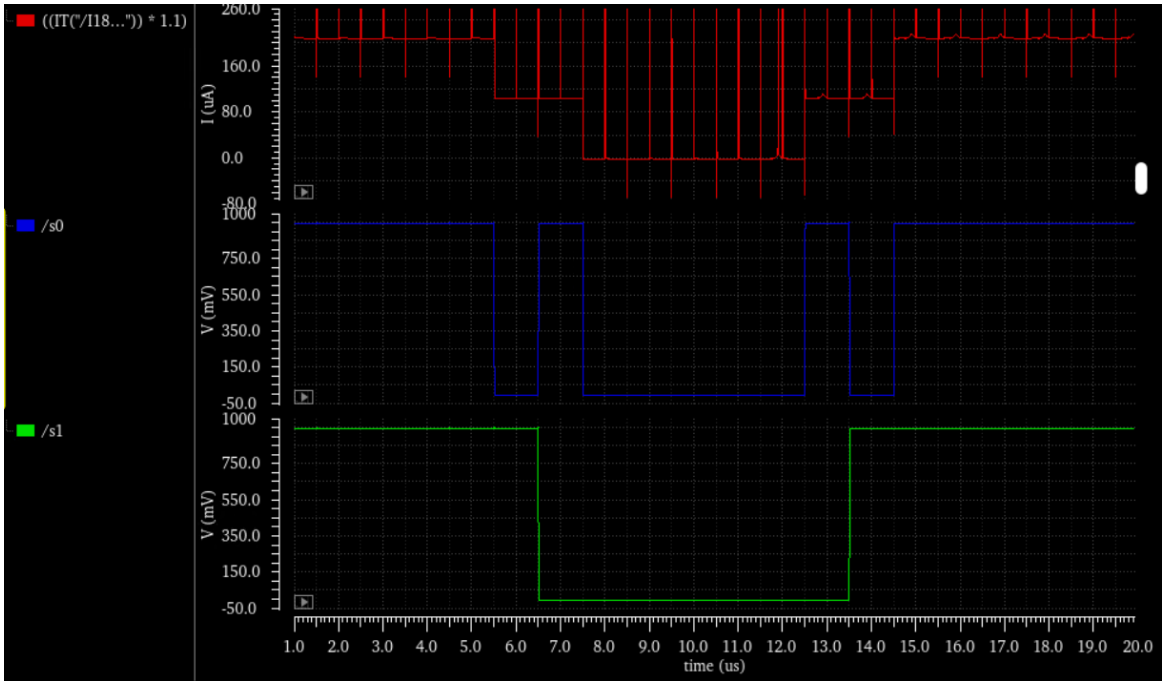

Figure 6.6: Instantaneous power consumption of the AGC.

summarised in Table 6.3. The table also includes the average power consumption when the FSM is in each state for an equal amount of time

6.4 Simulation of Amplification Stage

This section covers the simulation of the full amplification stage that includes the AGC, the TIA and the NIA (see Section 4, 5.4, and 5.5). The current coming in to the readout circuit from the REDOX reaction is represented by a DC current source. This current is swept in magnitude over a wide range to test how the AGC sets the gain of the TIA and NIA accordingly. The resulting simulation is displayed in Figure 6.7.

In the graph $I69/PLUS$ is the input current to the readout, *S1* and *S2* represent the state bits of the FSM, *dig_up* and *dig_down* are the respective outputs of the 'up' and 'down' comparators in the AGC, *clk* is the input clock, and TIA_OUT and OUT are the outputs of the TIA and NIA stages respectively.

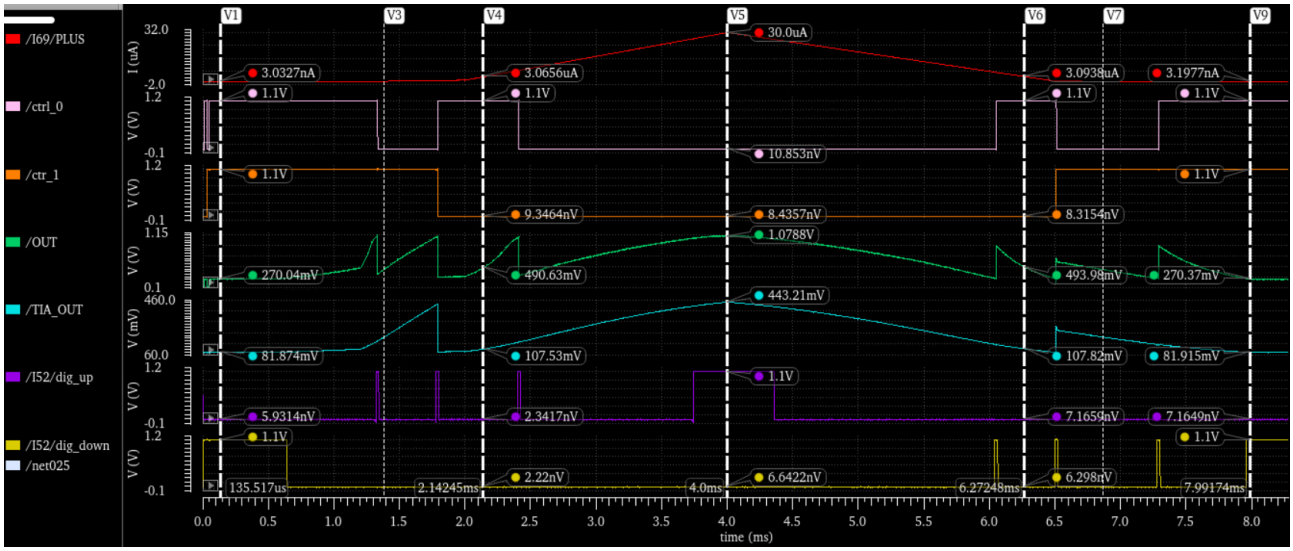

Figure 6.7: Simulation of amplification stage.

In the simulation, the input current is swept from $1nA$ to $30\mu A$ and then back to $1nA$ over a period of $8ms$. The simulation starts with the gain setting settled at the highest gain mode, as the input is of a low magnitude. As the input magnitude increases, OUT also increases and this causes the V_{UP} threshold of the upper comparator to be crossed, causing its output to go high. This causes the FSM to change state and reduce the gain, upon which the upper comparator output is able to go low again at the very next clock edge. Therefore this results in the short spikes in *dig_up* that are one clock cycle in length and can be seen in purple plot in the Figure. This happens until the AGC is not able to reduce the gain mode any further, resulting in *dig_up* going constantly high and the state bits both going to zero (mode of lowest gain). When the current is swept downwards the same happens with *dig_down* (seen in yellow plot). It spikes three times indicating the increase in gain and then stays high as the AGC is not able to increase the gain any more. At this point both the state bits are high (mode of highest gain).

The graphs shows that the system is capable of giving distinguishable outputs between $3nA$ and $30\mu A$. This is a considerably wide range of inputs giving the readout an input dynamic range of $80dB$.

The maximum average power consumption for the amplification stage was found for the case that both state bits of the FSM were high (Highest gain mode) as this is when the power consumption for the AGC is the highest (See Table 6.3). The average power consumption for the amplification stage was $\mathbf{584.6\mu W}$.

6.5 SAR ADC Simulation

The 8-bit ADC was tested using the transient analysis to observe its performance in various areas. The ADC was checked for various values of input voltage to check the accuracy of the 8 bit digital output code. To demonstrate its performance, the simulation for an analogue input of $700mV$ is presented in Figure 6.8.

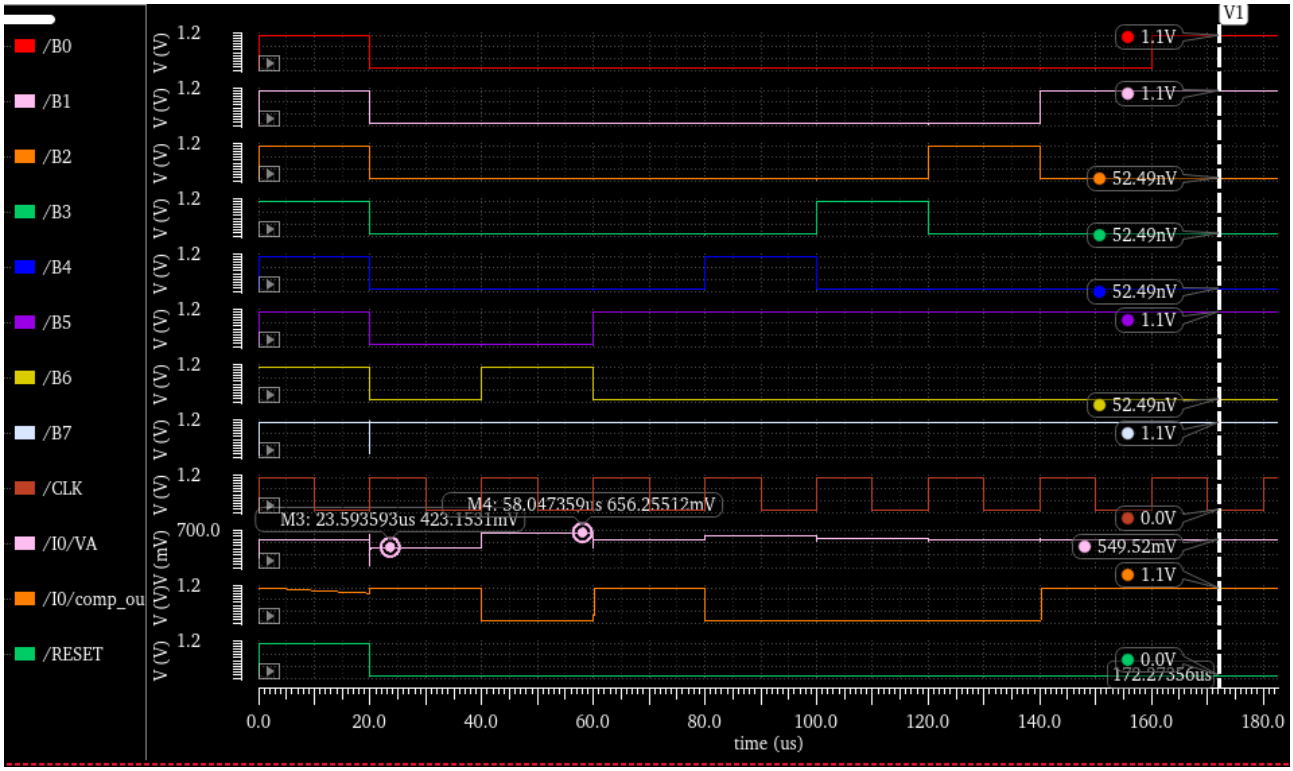

Figure 6.8: ADC performance with an input voltage of $700mV$.

BIT	BIT Voltage (mV)
B7	550
B6	275
B5	137.5
B4	68.75
B3	34.38
B2	17.19
B1	8.59
B0	4.30

Table 6.4: Bit weights (in mV) for each bit

In the Figure the sampling of the input happens when reset is high. V_A is the inverting input to the comparator and *comp_out* is the output of the comparator. As soon as reset goes low,

the operation of the SAR logic block starts and the MSB (B7) is set first. Since the input voltage is bigger than the MSB weight (see Table 6.4), V_A is less than $550mV$ and *comp_out* is high. The SAR logic block uses this to keep the MSB set when setting the next bit. When B6 is set, it can be seen that *comp_out* is low and so B6 is reset to zero. This procedure is carried on till all the bits are set and the conversion phase is complete. It can be seen that by the end of the conversion phase the bits that are set for an Analogue input of $700mV$ are:

$$B7, B5, B1, B0$$

This affirms that the ADC gives the correct output code for the input of $700mV$. Using the bit weights shown in Table 6.4, the equivalent digital output voltage is:

$$550 + 137.5 + 8.59 + 4.30 = 696.1mV$$

The error is therefore $700mV - 696.1mV = 3.9mV$ which is less than 1 LSB ($4.30mV$) as required. This error is present despite the correct output code of the ADC due to the limited precision of the ADC. The precision can be increased by increasing the number of bits of the SAR ADC, but this will increase power and area consumption. It was therefore deemed that 8 bits are sufficient for converting the input voltage accurately enough. A graph for the output code voltage versus the input voltage was also then plotted for the ADC and this can be found in the Appendix in Figure 11.9.

An error analysis was run on the ADC to observe how close the output code voltage of the ADC is to the input. The data was gathered on cadence and then exported to MATLAB where, the error graphs were plotted. Figure 6.9 shows the error of the ADC calculated using the error equation below:

$$Error_{LSB} = \frac{V_{OUT} - V_{IN}}{\text{Ideal LSB Width}}$$

where $Error_{LSB}$ is the error in LSBs and the ideal LSB Width is $4.3mV$ (see Table 6.4).

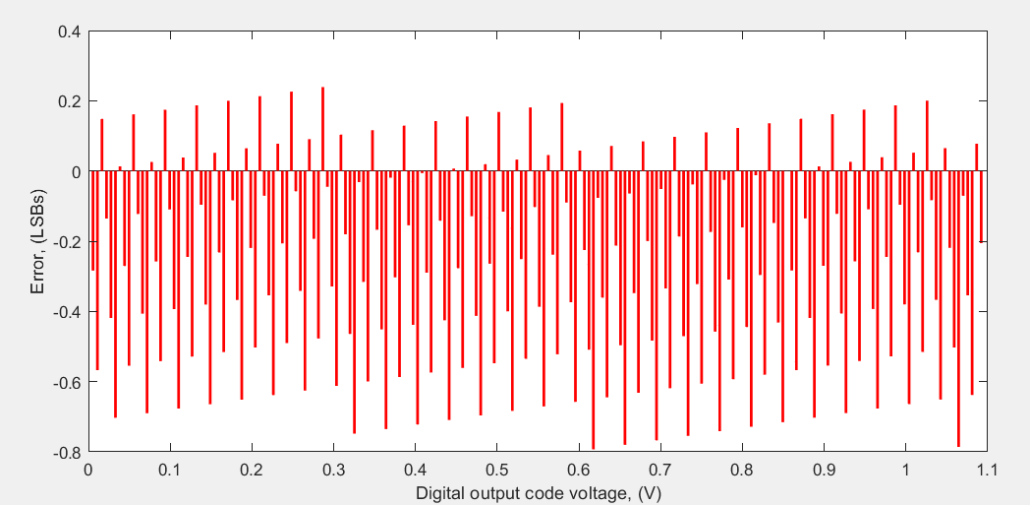

Figure 6.9: ADC Error.

It can be seen that there is a clear offset in the reading. The Offset in the ADC readings was found to be 0.2378 LSB. Once this was removed the ADC Error was run again and the resulting graph can be visualised in Figure 6.10.

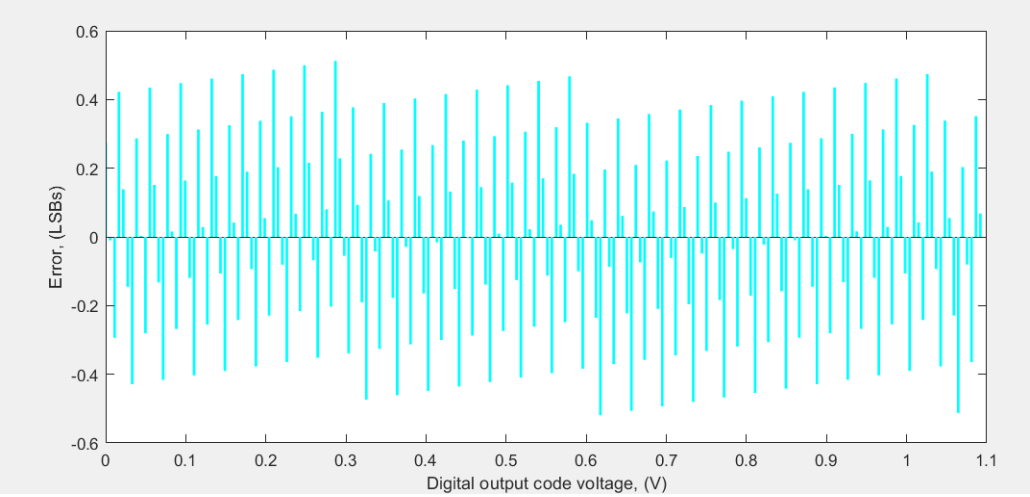

Figure 6.10: ADC error with offset removed.

The Error is always less than 1 LSB as expected verifying that the ADC is functioning in the desired way for the full output range of input voltages.

The ADC was found to have a worst case power consumption when the analogue input voltage was the lowest and so all the bits were set low. The average power consumption for the SAR ADC was found to be $\mathbf{55.02\mu W}$.

6.6 Full System Simulation

Finally, a full system test was run with the amplification stage and digitisation stage working together. Figure 6.11 shows the analogue output of the Amplification Stage plotted with the digital output of the Digitisation Stage.

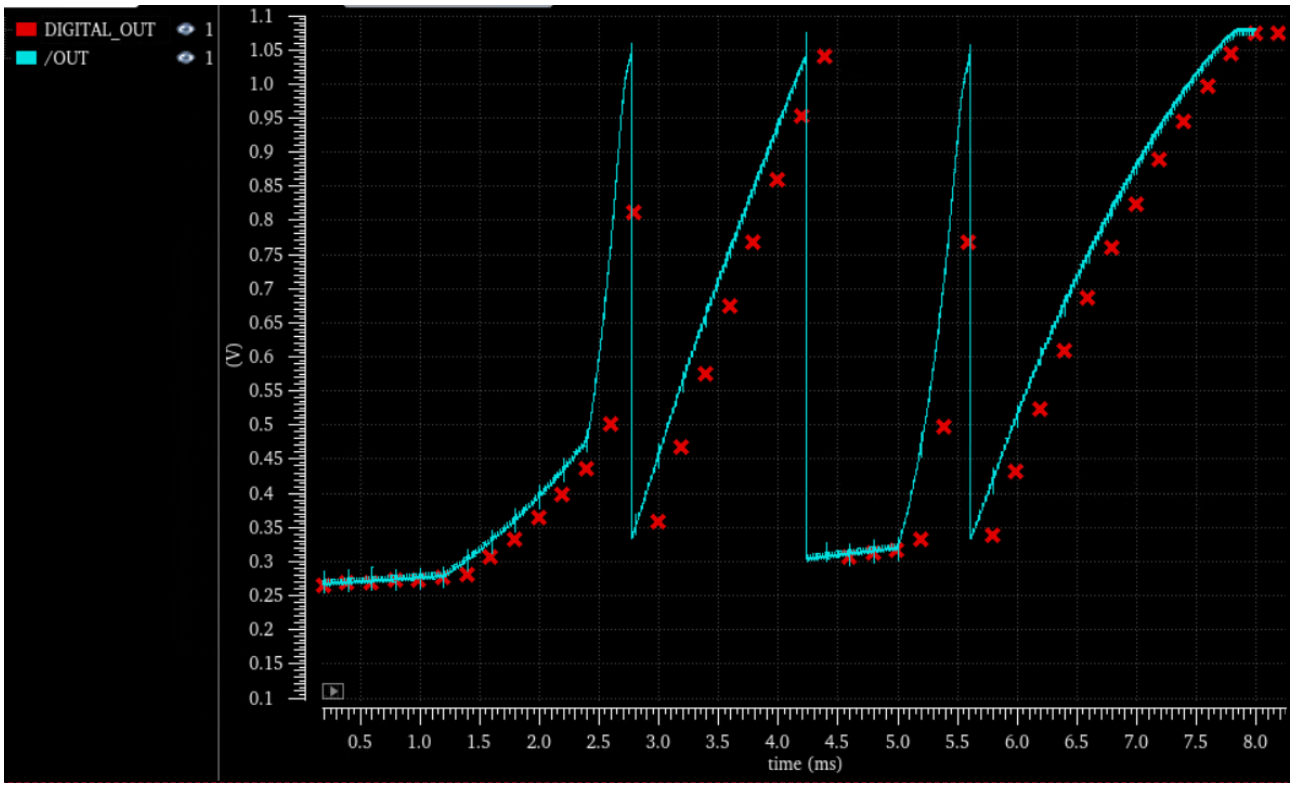

Figure 6.11: Output of Amplification Stage (blue) and Digitisation Stage (red).

The simulation is run with the input current swept from $1nA$ to $30\mu A$ over a period of $8ms$. The Figure shows that Digital Output closely follows the Analogue output. There is an expected delay about $200\mu s$ ($10 \times 20\mu s$ clock periods) between the analogue and digital signals. Even though the ADC is able to capture the general features of the analogue signal, an even better representation can be formed by just increasing the clock frequency. However, ADC parameters may need to be adjusted accordingly for this to be possible.

The total average power consumption of the entire readout circuit while it is operating in high gain mode was then found to be $\mathbf{670\mu W}$. When the circuit is not operating in the highest gain mode, the average power consumption reduces by up to $200\mu W$.

7 Results discussion

7.1 AGC settings

7.1.1 Setting of clock frequency

Selection of the appropriate clocking frequency is important as it can affect the operation of the AGC unit. The AGC was simulated for several different clock periods in order to determine the optimal range of operation. From the results of the simulation, it was apparent that there was an inherent trade-off for selecting clock periods. This is summarised in Table 7.1.

Short Clock period (High Frequency)	Long Clock Period (low frequency)
• Total delay from the gate logic shown in Figure 11.1 becomes more significant as the clock period reduces. If the gate delay becomes long enough to be comparable to the input clock frequency, it could mean the incorrect gain mode is set and the AGC outputs could oscillate. • Comparator operation is affected as it is unable to process its inputs when the clock frequency is too high. • Dynamic power consumption increases as the clock transitions cause spikes in current. The power consumption of the dynamic comparator is also directly proportional to the frequency of the clock. Therefore average power consumption also increases.	• A higher clock period means an increased amount of time for the AGC to set the gain mode, which could result in important features of the input being missed. • Output voltage may start clipping the power rails before the gain is able to be set accordingly, resulting in loss of information. • Another issue is the reduced throughput of the system meaning that less information would be sent out of the readout due to the limited clock frequency. However, if the clock frequency is still high enough to capture fast varying biomedical signals, then this would not be a problem.

Table 7.1: Comparison of AGC with different clock periods

It was found that the FSM and the AGC circuitry were able to function properly when the clock period was $\geq 1\mu s$ ($\leq 1MHz$). It was initially decided to set the clock frequency to $500kHz$, however, it was needed that the clock frequency of the AGC aligned with the working clock frequency of the SAR ADC. Therefore, it was finally decided to have a clock with a period of $20\mu s$ ($50kHz$) for the entire readout circuit. This was appropriate because

the AGC was fully functional at this clock frequency and the clock frequency was still high enough to capture the relatively slow varying biomedical signals.

7.1.2 Setting of comparator thresholds

The setting of the V_{up} and V_{down} thresholds for the up and down comparators needed to be done carefully as this had a direct impact on the readings. Table 7.2 compares having the thresholds wide apart (higher V_{up} and lower V_{down}) versus having the thresholds close together (lower V_{up} and higher V_{down}).

Wide Threshold Range	***Narrow Threshold Range***
• Having the thresholds spaced wide apart means that a wider range of inputs can be uniquely measured in the same gain mode. In other words, the input can vary more before the AGC circuitry increases or decreases the gain mode. Therefore this results in an increase in the input dynamic range.	• Having the thresholds closer together will offer protection against the fast changing inputs. For example, if the input changes faster than the AGC can change the gain mode, it could result in the voltage clipping the power rails, resulting in inaccurate communication of information. If the thresholds of the comparators are placed far enough from the voltage of the power rails, this problem could be mitigated as it would offer more time for the voltage to change before the AGC changes the gain mode • The dynamic comparators in the AGC do not operate properly for the full range of input voltages. Their operation starts to be affected when the voltages at at least one of their inputs approach V_{DD} or ground. It was found after simulation that these comparators only work properly for an input voltage range (for at least one input) of $250mV < V < 1000mV$. Therefore both 'up' and 'down' thresholds need to be within this range. • The NIA amplifier adds an offset of about $265mV$ to the output that must be considered. Therefore the V_{down} comparator threshold voltage must also be above this limit.

Table 7.2: Comparison of comparator thresholds wide apart versus closer together.

Considering the information presented in Table 7.2, the threshold voltages for the up and down comparators was set to $950mV$ and $290mV$ respectively.

7.2 SAR ADC challenges

Two major problems of charge leakage and the comparator threshold must be taken into account. In this section, we discuss how these issues can be addressed.

Initially the SAR ADC was developed in the way shown in Figure 2.9, with the non-inverting input of the comparator set to a ground reference. Once the sampling phase completes and the MSB is set to start the comparison, a large negative voltage of up to $\frac{-V_{DD}}{2}$ $(-550mV)$ could appear at the inverting input of the comparator. This was problematic because the switches used were not able to maintain this large negative voltage and so charge would leak through these switches, reducing the magnitude of the negative voltage and hence resulting in an incorrect conversion. This problem would worsen with larger values of V_{IN} as this meant a higher negative voltage at the inverting input. The solution to this was to bias the non-inverting input of the comparator with a common mode voltage V_{CM} set to $550mV$ as shown in Figure 5.7. In this way all the voltages were offset by $550mV$ and so the lowest possible voltage at the inverting input with this configuration was $0V$. So the problem of negative voltage and hence charge leakage was removed.

Biasing the non-inverting input at the $550mV$ instead of ground also significantly improved the comparator operation. With ground as a reference, one of the differential pairs of the double cascode comparator (see Section 5.8) was always off ($V_{GS} << V_{TH}$), while the other was also impacted by low voltages. This severely affected the open loop gain of the comparator as it was unable to amplify small differences in the input, and so the correct bits could not be set by the SAR logic block. Biasing the Comparator at $550mV$ meant that both the differential pair transistors can maintain a high enough V_{GS} to enable the comparator to function appropriately.

7.3 Full System Results

The 8-bit output of the ADC, along with the 2 bits representing the gain setting need to be communicated to an external device. The values received by the external device are to be compared against stored set of previously measured results in order to determine the concentration of the target analyte in the electrochemical solution. Therefore, once the initial measurements are collected and stored for comparison, there should be limited reason to perform any further calibrations on the readout.

8 Layout

The layout of the designed readout circuit was done, and this is shown in Figure 8.1. The layout done includes all components strategically placed and routed.

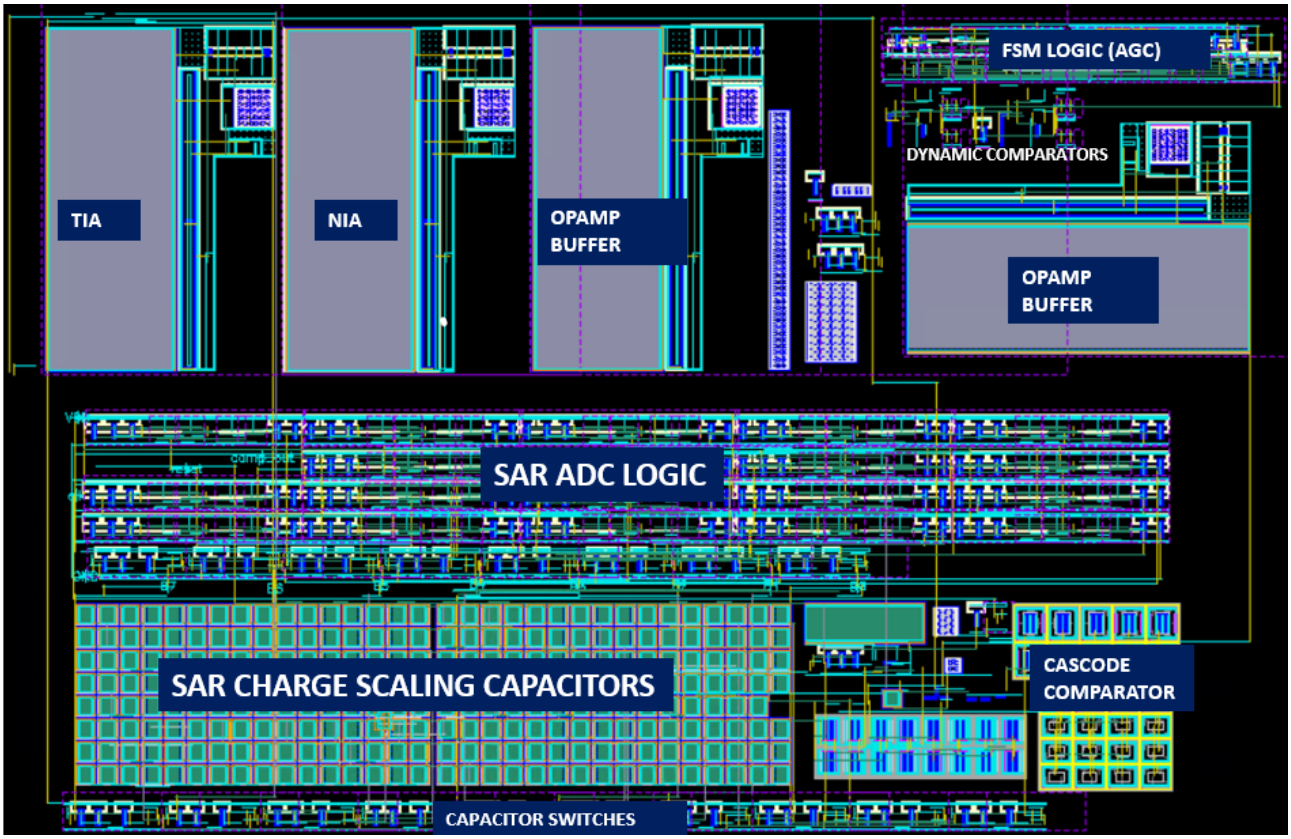

Figure 8.1: Full Layout view of readout circuit.

In the layout it can be seen that the digital circuitry, the SAR ADC and the AGC, are kept a distance apart from the analogue circuitry. This helps to improve noise performance of the readout. The digital circuitry in the SAR ADC logic block and in the FSM is laid out longitudinally. It can be seen that the capacitors are the components that take up the most amount of space. The dynamic comparators shown near the top right of Figure 8.1 are found to be significantly smaller in terms of total area consumed as compared to the cascode comparator shown at the bottom right. This is another comparative advantage of their use in addition to the lesser power consumption (see Table 6.2).

The full layout cell was found to be $290\mu m \times 440\mu m$ in dimensions.

9 Evaluation

This section evaluates the performance of the design with two metrics:

1. According to the initial objectives of the project laid out in Section 3.
2. According to specifications of other similar readout circuits presented by other authors.

9.1 Evaluation of design with objectives

It is important to evaluate the design with previously laid out objectives in order to understand how much and to what extent were the goals of the project fulfilled. It also gives an insight on how the project can be improved upon.

⇨ Autonomous: The readout circuit developed employs an FSM based automatic gain control (AGC) unit than can respond to inputs of varying magnitudes by dynamically changing with gain. In this way, the readout circuit is able to have a wide dynamic range of about $80dB$ by employing only four different gain levels. Therefore, external intervention from needing to manually calibrate the readout circuit parameters to respond to different inputs is greatly reduced. As discussed before, this is an extremely desirable feature to have for implanted devices as repeated external action can cause irritation and harm to the patient.

⇨ Compact: As mentioned in Section 8.1, the dimensions of the of full design are $290\mu m \times 440\mu m$. This is compact enough to fit on minuscule implantable device allowing the full system to be minimally invasive. Further improvements, however, can be made to make the size of the layout even more compact.

⇨ Low Power: The designing of all the components was done carefully to achieve the specifications needed while minimising the power consumption. A comparatively low supply voltage of $1.1V$ was used to further reduce power consumption, even though this made the biasing of components more difficult. Components with lower power consumption were preferred wherever possible such as in the case of the AGC where the dynamic comparator was used instead of the double cascode comparator. Such techniques allowed a low power readout circuit to be developed with an average power consumption of $670\mu A$, well within the set power budget of $1mA$.

⇨ Robustness and reliability: The readout was simulated for the full range of expected inputs ($3nA - 30\mu A$) to make sure it was operational in this input range. Voltage thresholds for the comparator in the AGC were carefully selected (see Section 7) so that fast changing inputs could be measured without the voltage at the output of the amplification stage clipping the power rails. The SAR ADC was developed to convert the reading into a digital signal for communication. Since digital signals are less susceptible to noise, this ensured more reliable communication.

⇨ Diversified, selective and accurate: This feature is meant to be acquired once electrodes for the system are developed in the way described in Section 2.3. It is left to future collaborators to explore this avenue and incorporate it into the readout circuit presented in this report.

9.2 Evaluation of design with other works

This section helps provide a broader understanding of this work in comparison to the previous works in the literature. Table 9.1 shows the comparison of the specifications of this readout circuit with other state of the art readout circuits.

Paper	**Technology (μm)**	**Supply Voltage (V)**	**Dynamic Range (dB)**	**Power (mW)**	**Gain Modes**	**Autonomous Adjustments?**
[32]	0.35	3.3	83	0.190	2	NO
[39]	0.5	3	134	1.27	9	NO
[26]	0.5	5	164	0.241	4	NO
[21]	0.35	3.3	153	9.30	4	NO
[27]	0.5	3.3	84	0.021	2	NO
[20]	0.35	3.3	169	5.83	8	YES
[12]	0.18	3.3	120	13.86	-	YES
This Work	0.18	1.1	80	0.670	4	YES

Table 9.1: Comparison of readouts circuits [12, 20]

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10 Future Work and Conclusion

The design presented in this report can provide a foundation for several other works. Several aspects of the project can be further improved allowing the system to be even more versatile. Some of the future work is listed below:

- *Offset removal schemes:* The offset at the output of the NIA leads to a reduction in dynamic range of the readout. Therefore future works can include the use of several offset removal schemes such as differential handling of the signal and auto-zeroing. Rail-to-rail output opamps based on folded cascode topologies can also be explored to help increase dynamic range.
- *Communication and PMU:* Additional circuitry to wirelessly power the system needs to be added before the fabrication. Circuitry also needs to be developed to communicate the digital output bits of the ADC and the state bits from the FSM to an external storage or data processing system.
- *Electrodes and Potentiostat:* The design and fabrication of electrodes and potentiostat circuitry in the ways discussed in previous sections is also highly recommended to be explored by future participants. Once this is done, the full electrochemical sensing system can be fabricated and tested altogether for its performance in a real environment.
- *Increasing Gain modes:* Increasing the number of gain modes means that a the readout can respond to a wider range of inputs. In order to implement this, extra bits will need to be added to the FSM and the logic needed to drive them can be derived using the methods detailed in Section 5.5. Adding an extra bit will result in twice the number of gain modes but can increase power consumption by up to a $100\mu W$ per bit added. The transimpedence and non-inverting amplifier gains will then also have to be adjusted accordingly.
- *SAR ADC improvements:* The charge scaling capacitive DAC in the SAR ADC consumes a significant amount of space as the MSB capacitor needs to be 128 times larger than the LSB capacitor. This can be improved using split array techniques detailed in [9]. This can make the SAR ADC and the overall circuitry noticeably more compact, however, issues can arise when if bit weights are not properly balanced. Additional bits can also be added to the SAR ADC that can help reduce the systematic error of the ADC caused due to the LSB bit voltage being too high. Each additional bit added will reduce the maximum systematic error by half. However, as more bits are added, random errors from noise might start to get increasingly significant.

This report presents a readout circuit with an autonomous gain control unit and a SAR ADC that achieves a unique combination of specifications compared to other similar works as seen in Table 9.1. It offers a wide 80dB worth of input dynamic range achieved by using four distinguishable gain modes. It is able to operate on a low voltage and low power supply of $1.1V$ and $670\mu W$ respectively. The FSM based AGC circuit is able to accurately set the gain of the amplification stage according to the input magnitude. The 8-bit SAR ADC operates at a low power of $55\mu W$ and achieves a precision of less than one LSB ($4.3mV$) for all inputs (Section 6.5). A compact layout for the readout was then also presented in Section 8.1, with dimensions of $290\mu m \times 440\mu m$.

Several unique but simple solutions were cleverly used to tackle several challenges faced along the way. The change of gain for the TIA and the NIA was cleverly employed by adding a switch in the path of one of the resistors connected in parallel. Since the two resistors were connected were very different in size, the closing and opening of the switch conveniently changed the gain of this parallel combination of resistors and hence altered the gain of the TIA and NIA (Section 5.4). For the SAR ADC, the V_{CM} biasing of the comparator alleviated all issues by removing the need to support low and negative voltages, as discussed in Section 7. A bootstrap switch was also presented in Section 5.9 and was used to allow the sampling of the input voltage with minimal offset added due to charge injection.

To summarise, this document provides a unique insight into the development of a compact, low power autonomous readout circuit and is hoped provide a foundation for future works in this field. Undertaking this project made me understand the vast possibilities of CMOS ICs used in biomedical applications. I learnt that with the right knowledge and equipment, one can design a tangible system that can in actuality go towards easing the lives of people. This prospect excites me even more about the many applications of the biomedical technology and I hope to undertake a similar feat as this project in the future.

11 Appendix

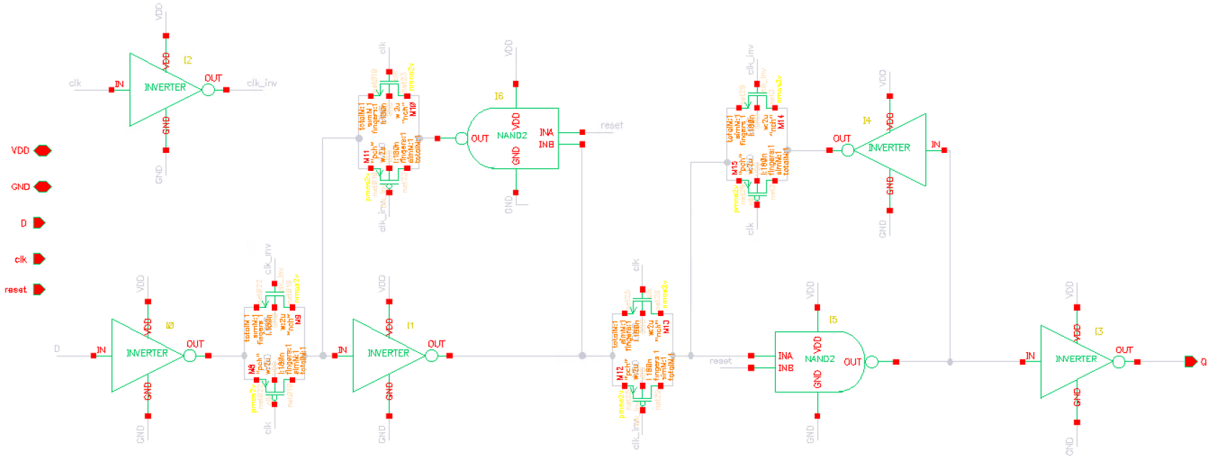

Figure 11.1: DFF.

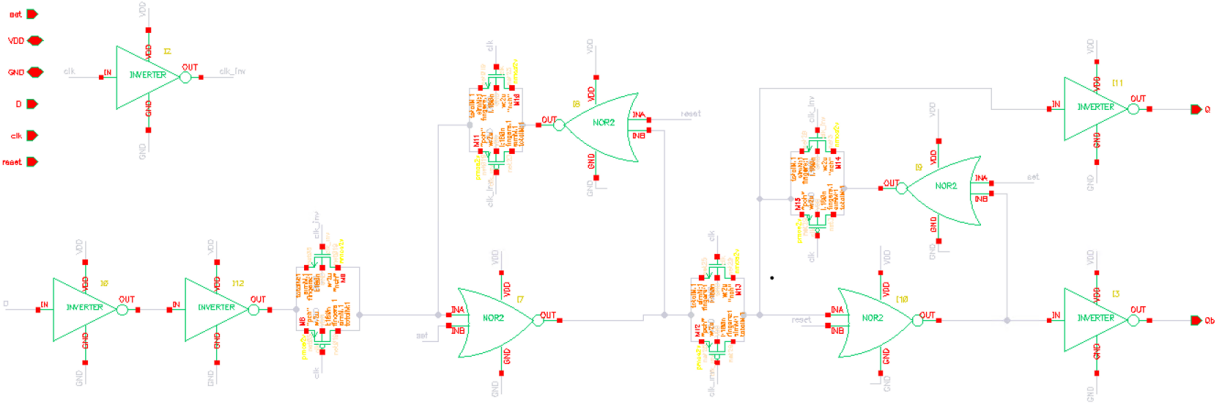

Figure 11.2: DFF with asynchronous set and reset.

Up	Dn	S1	S0	S1+	S0+
1	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	0	0
0	1	0	1	1	0
1	0	1	0	0	1
0	1	1	0	1	1
1	0	1	1	1	0
0	1	1	1	1	1

Figure 11.3: State Transition Table for AGC FSM.

For S0+

UpDn/s1s0	00	01	11	10
00	0	1	1	0
01	1	0	1	1
11	x	x	x	x
10	0	0	0	1

S0+ = S1'S0'Dn + Up'Dn'S0 + Up'DnS1 + S1S0'Up

Figure 11.4: KMAP for S0 output of AGC FSM.

UpDn/s1s0	00	01	11	10
00	0	0	1	1
01	0	1	1	1
11	x	x	x	x
10	0	0	1	0

S1+ = DnS0 + Up'S1 + S1S0

Figure 11.5: KMAP for S1 output of AGC FSM.

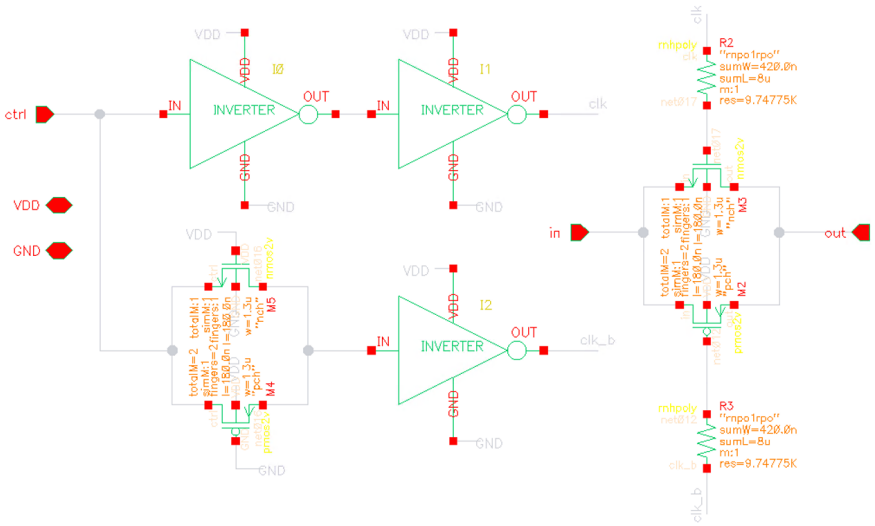

Figure 11.6: 2 terminal analogue switch.

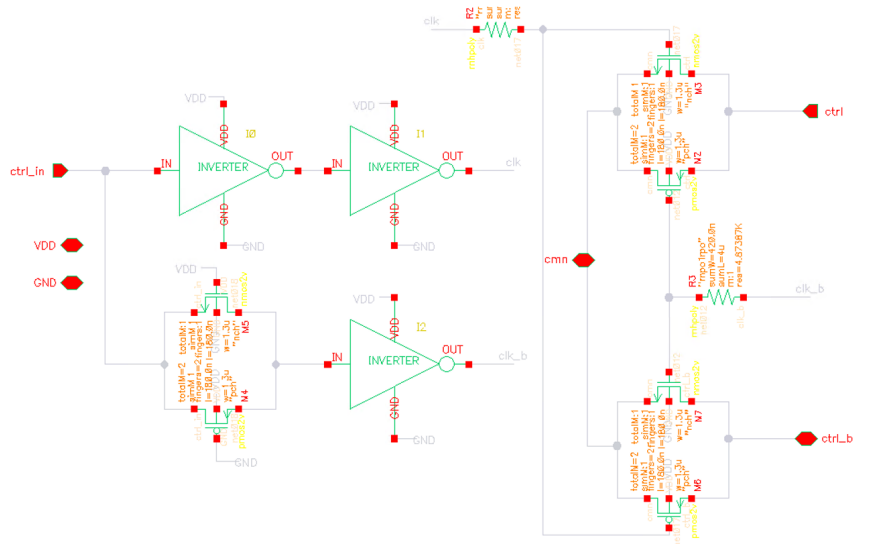

Figure 11.7: 3 terminal analogue switch.

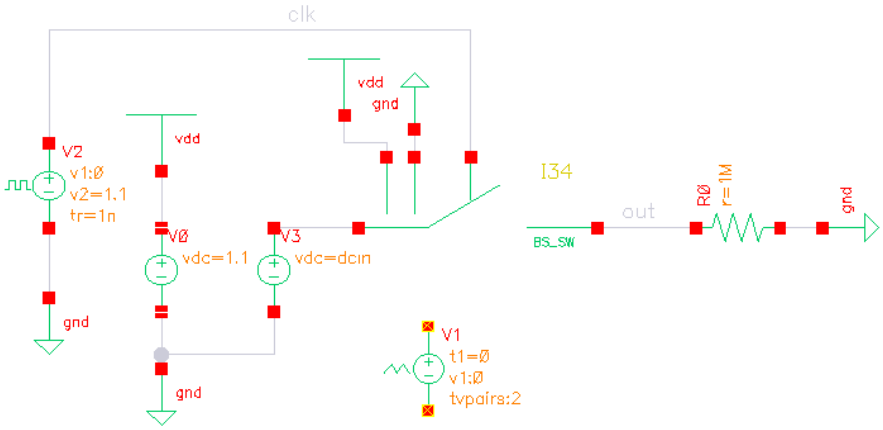

Figure 11.8: The bootstrap switch testbench schematic.

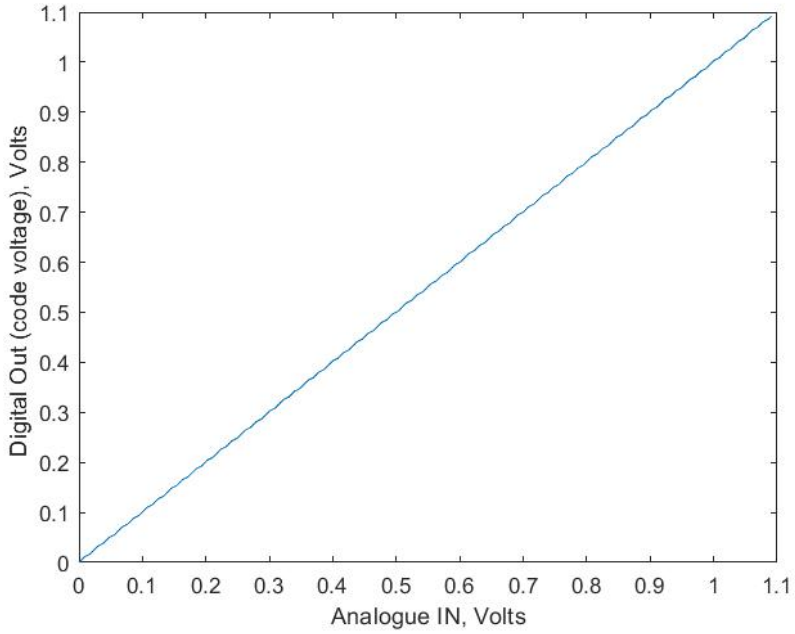

Figure 11.9: SAR ADC Output code voltage vs. Analogue input voltage (plotted on MATLAB).

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