A Wireless Power Management Unit with a Novel Self-Tuned LDO for System-On-Chip Sensors

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***Abstract*—A wireless power management unit is presented in this work. The system size of 0.4mm^2 with the low power consumption of 87μW allow it to be applied in implantable biomedical applications and ex-vivo systems. The proposed system optimises the conventional slew-rate detection low drop-out (LDO) circuit by using a self-tuned controlling block that reduces the response time to 100ns. The static power required for this LDO is reduced to 2μW. The band gap reference (BGR) is designed with a high power supply rejection ratio (PSRR) of 60dB at 100kHz, along with an output reference voltage deviation of 1mV, to deal with the power supply ripple caused by the load shift keying (LSK). The RF power is transmitted at 433MHz and the internal power management circuit is able to provide a 1.4V stable DC supply for a front end on-chip sensor.**

***Index Terms*—Wireless Power Transfer, LSK, LDO, BGR, low power**

I. Introduction

Wireless power transfer (WPT) technology has advanced rapidly over recent years with a growing number of applications [1]. Besides traditional usage in phones, laptops and vehicles, biomedical devices are well-placed to utilise this technology for building wireless connections between the human body and external circuits [2]. Furthermore, power transfer from circuits external to the body to in-vivo systems for implanted devices removes the need for a rechargeable battery [3]. As a result, invasive wires are unnecessary and the lifetime of the application would not be limited by the small batteries.

A power management unit (PMU) is necessary for the implementation of an efficient WPT system. Many research groups have worked towards improving the PMUs. Peng et al. proposed a rechargeable battery-operated biomedical application powered by a rechargeable battery and external wireless power [4]. Shun et al. introduced an active capsule endoscope with high power consumption motors [5]. However, these units have very large off-chip capacitors and resistors which require extra post-processing work compared to a system-on-chip circuit. Mohammad et al. employed two separate power transmitters to stabilise the PTE of the PMU [6]. Cheng et al. invented a new active rectifier, capable of providing different voltages, to maximise the PTE by reducing the number of system stages [2].

These prior works are implemented with comparably complex systems and larger areas, which are unsuitable for miniaturised system-on-chip designs. This paper presents a simple low-power wireless power management system. The data detected by the sensor is transferred wirelessly through a LSK circuit. This LSK circuit also causes a voltage ripple at the secondary side coil, which modulates the supply voltage for the front end sensor. The proposed system utilises a novel self-tuned LDO to mitigate the voltage fluctuation from previous stages.

The rest of this paper is organized as follows: the section II introduces the operational principle of the system and demonstrates the novelty of this architecture. Section III details the circuit implementation. Section IV illustrates the simulation results. Section V concludes this work.

II. System Architecture

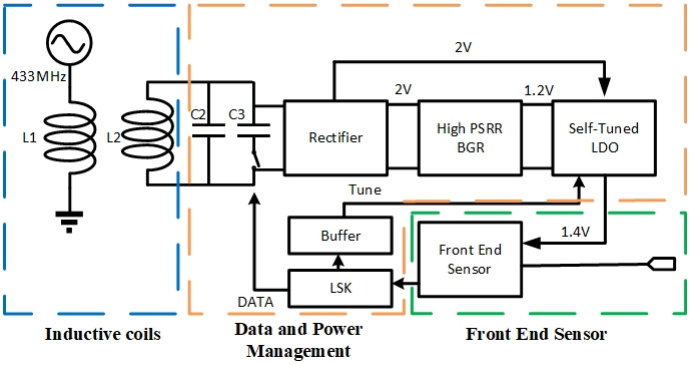

Fig. 1. The system consists of three blocks: Inductive coil, data and power management, and front end sensor. The secondary coil L_2 receives wireless power from the external circuit and feeds this AC power to a rectifier. A high PSRR BGR after the rectifier is responsible for providing a stable voltage for the self-tuned LDO circuit, which is capable of down-converting the 2V supply to a regulated 1.4V voltage supply for front end sensor.

The system architecture is shown in Fig 1. The inductive coils are designed and manufactured at a working frequency of 433MHz with a maximum PTE of 19.2% [7]. The secondary coil L_2 receives wireless power from the external circuit and feeds this AC power to a bulk-regulated rectifier, whereby it gets converted to a DC supply with the help of a smoothing capacitor. A high PSRR BGR after the rectifier provides a stable 1.16 reference voltage for the self-tuned LDO circuit. The LDO finally down-converts the 2V DC supply to a regulated 1.4V voltage supply for front end sensor.

A voltage fluctuation is generated at the secondary coil due to the LSK circuit. The modulation of the resonant frequency of the inductive coils deteriorates the stability of the BGR

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and LDO. To circumvent this, a large valued 300pF capacitor at the rectifier output is utilised at the cost of a large area. Additionally, a high PSRR BGR is necessary to provide a stable reference voltage. A novel self-tuned LDO is also proposed in this work to stabilize the 1.4V output voltage supply and reduce the power consumption.

III. CIRCUIT IMPLEMENTATION

The prototype is developed using TSMC180nm technology, and each circuit block is detailed below.

A. Bulk Regulated Rectifier

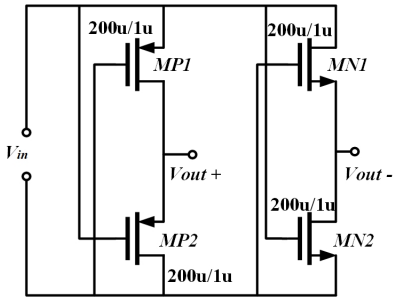

Fig. 2. Fully cross-coupled rectifier.

A rectifier converts the received AC voltage to a DC voltage, and provides a power supply for the rest of the circuit. The conventional rectifiers are usually implemented by diodes, which are not suited in standard CMOS techniques [2]. In this work, the rectifier is implemented by using a fully cross-coupled structure as shown in Fig. 2 [8]. The principle behind this is that in each half cycle of the period, either MN1 and MP2 or MP1 and MN2 are turned on, forcing the output node Vout+ to always be higher than Vout-. This circuit has an advantage of a low voltage drop caused by two V_{ds} in each CMOS branch (expressed in equation 1), rather than threshold voltages of diodes in conventional rectifiers. Hence, a high voltage conversion ratio is achieved.

$$V_{\text{loss}} = V_n + V_p = \sqrt{\frac{2I_d L_n}{\mu C_{ox} W_n}} + \sqrt{\frac{2I_d L_p}{\mu C_{ox} W_p}} \approx 0.4V \quad (1)$$

However, this rectifier shows a low power conversion efficiency of 60% at working frequency of 433MHz [7] due to flow back current.

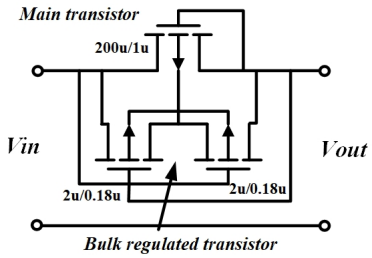

Fig. 3. Bulk regulated circuit. It should be connected to all the transistors in the rectifier.

For mitigating the body effect, the bulk terminal of each transistor should always be connected to its source terminal. Thus, a bulk regulated circuit is applied to each transistor at a cost of the increased area. This circuit works such that among the two bulk regulated transistors, only one transistor connected to the lower voltage potential is turns on, ensuring the main transistor's bulk is connected to its lower potential side. This is shown in Fig. 3.

B. High PSRR Band Gap Reference

A conventional BGR is formed by using a PTAT current generated by base-emitter junctions of a BJT, and a CTAT voltage drop across diodes [9]. However, this conventional BGR has a low PSRR, which means the stability of the output reference will be badly deteriorated by the power supply ripples caused by the LSK. The PSRR of a conventional BGR can be expressed in equation 2 [7],

$$PSRR = \frac{v_{\text{ref}}}{v_{\text{dd}}} \propto \frac{1 - PSRR_{\text{opamp}}}{A} \quad (2)$$

where $PSRR_{Opamp}$ is the PSRR of the opamp and A is the gain. It indicates that if the opamp follows the ripple of power supply, the PSRR of the BGR will theoretically be infinite [10]. Thus, a high PSRR BGR can be designed. Based on this idea, a schematic is shown in Fig. 4.

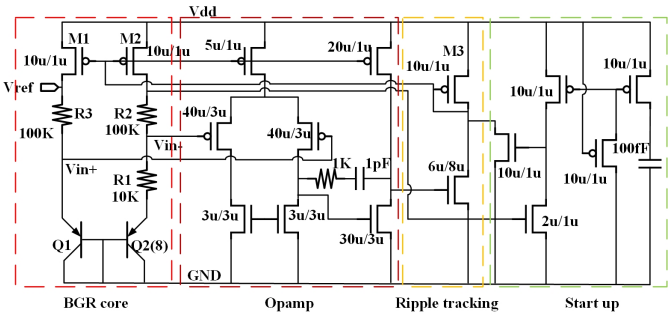

Fig. 4. The High-PSRR BGR schematic consisting of four parts - the core, opamp, ripple tracking and start up circuits.

This circuit is composed of four parts. The bandgap core provides a temperature independent voltage by combining a PTAT and a CTAT voltage:

$$V_{out} = V_{be1} + \frac{R_2}{R_1} V_T \ln(8) \approx 1.2V \quad (3)$$

The opamp forces its two input nodes $Vin+$ and $Vin-$ to the same potential, ensuring the current flowing through R1 and R3 is fixed through the current mirrors M1 and M3.

A ripple tracking block is added after the opamp. This consists of a diode-connected PMOS M3 in series with a common-source NMOS that feeds the supply ripple from its source terminal directly to its drain and gate terminals. Thus, the output of this opamp tracks the supply ripple, fixing the source-gate voltage of M1 and M2. The channel length modulation is neglected by using long channel length PMOS M1 and M2, ensuring the drain current will not be affected by

Vds. As a result, the current flowing through M1 and M2 is always fixed regardless of the power supply ripple as described in Fig. 5. Lastly, a startup circuit enables M1 and M2 to work in the saturation region during the power on stage. The PSRR of this BGR achieves -86dB at 10kHz and -60dB at 100kHz.

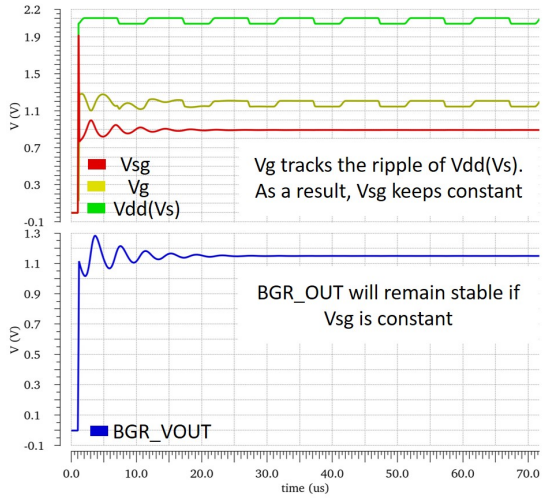

Fig. 5. The waveform of the High-PSRR BGR. The current mirror gate terminal voltage (Vg) follows the ripple of the source terminal voltage (Vs), ensuring V_{sg} remain constant. As a result, the voltage output reference keeps constant regardless of the power supply ripple.

However, it is important to note that this ripple tracking block along with the two-stage opamp forms a three-stage opamp, possibly deteriorating the stability of the overall circuit. In addition, the transistor M5, M4, M3, M6 form local positive feedback, which may potentially lock the circuit and shut it down. Thus, the second and third stage gain should be reduced to slow down this local positive feedback.

C. Self-Tuning Low Drop Out circuit

LDO circuits convert the supply to a relative low level, hence minimizing the system power consumption. However, conventional LDO circuits suffer from slow response times, slow slew rates and low bandwidths. Recently, different techniques have been proposed to resolve these defects [11]–[13]. Most of these techniques utilize slew rate detection at an internal node to boost the current when the input voltage changes. However, these are not suitable for systems with miniscule changes in the input voltage.

In order to resolve this issue, a novel self-tuned LDO that works with a 50mV input ripple is proposed. This is shown in Fig. 6.

The self-tuned controller boosts its current once Vin changes. In this system, Vin of the LDO comes from the output voltage of the rectifier with a ripple of 50mV caused by the LSK. This digitized LSK data from the front end sensor can also be used to tune the LDO circuit. In order to decrease power consumption at steady state, the digitized data is connected to a high pass RC circuit, and boots the biasing current for a very short time but just enough to stabilize the

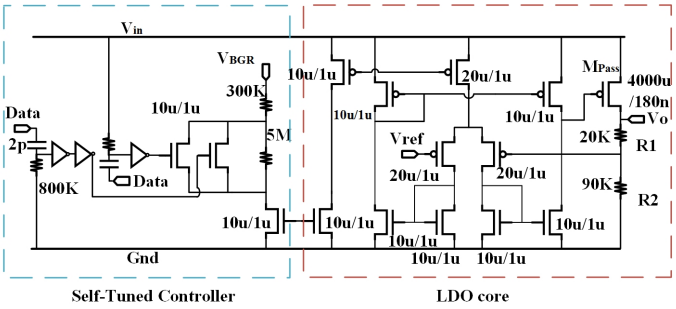

Fig. 6. The proposed self-tuned LDO circuit with a biasing block and core blocks.

LDO output. The slew rate increases with the increased biasing current, while response time is also reduced as shown in the Fig. 7.

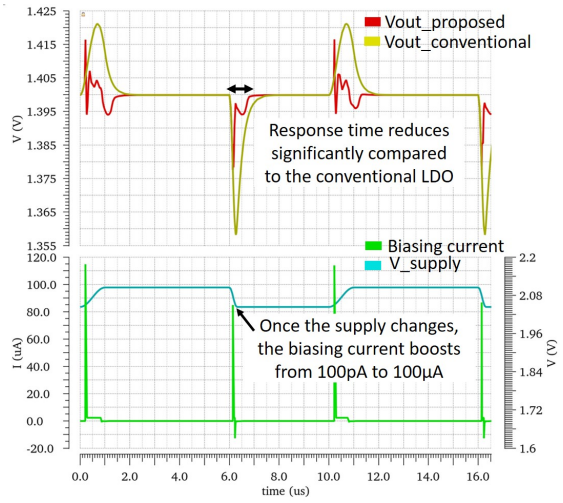

Fig. 7. Simulated line transient response of the conventional and the self-tuned LDO circuit. The response time reduces from 1.5μs to 100ns for negative supply change, and 2μs to 1μs for positive supply change.

As Vin changes from 2.11V to 2.04V, the static current increases from 100pA to around 100μA, dramatically reducing the response time from 1.5μs (yellow line) to 100ns (red line). For a positive supply change from 2.04V to 2.11V, the response time reduces from 2μs to 1μs. The proposed LDO reduces the ripple from 20mV to 5mV as well.

However, the proposed LDO requires precise latency control between LSK data and the input supply. All the other supply voltage interference was ignored, which may also potentially cause output instability.

IV. SIMULATION RESULTS

Fig. 8 shows the system layout diagram of the system. The circuit will be fabricated using TSMC 180nm technology. All the system characteristics are summarised in Table I, and the comparison with other state-of-the-art WPT system is concluded in the Table II.

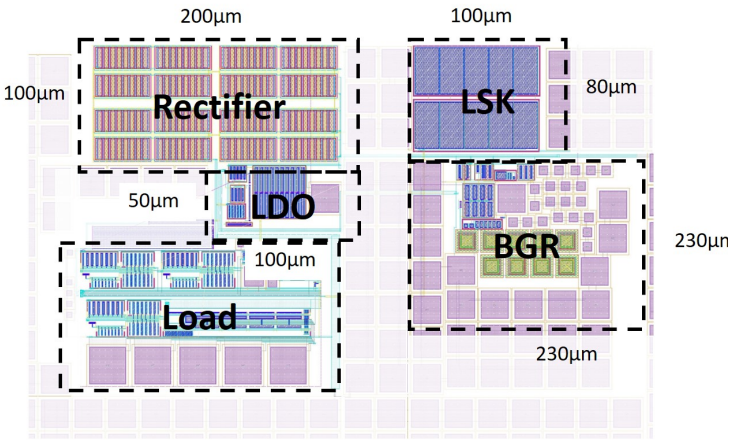

Fig. 8. System Layout diagram. The individual core electronic blocks are detailed, along with their dimensions.

TABLE I
SYSTEM CHARACTERISTICS SUMMARY

Parameter	Performance
System:	
Technology	TSMC $0.18\mu m$
Supply voltage(external circuit)	2.4V
Data transmission technique	LSK
Coil dimension	$3mm \times 3mm$
WPDT system dimension	$936\mu m \times 426\mu m$
Power dissipation (WPDT)	$87\mu W$
Rectifier:	
Area	$200\mu m \times 100\mu m$
Power efficiency	60%
Voltage conversion efficiency	90.9%
BGR:	
Area	$230\mu m \times 230\mu m$
Supply Voltage	$> 1.9V$
PSRR	$-90dB@ < 30KHz$ $-60dB@100KHz$
Power consumption	$61\mu W$
Output Voltage	$1.16V$
LDO:	
Area	$100\mu m \times 50\mu m$
Response time	$100ns$
Power consumption	$2\mu W$

For a simulated 300kHz data transmission, the voltage shift detected at the primary side is around 1V - which is large enough to be recovered. The supply ripple from the rectifier is around $50mV$, while the voltage fluctuation at the BGR is only 1mV.

The maximum efficiency of the rectifier can be achieved at 60% when the W/L of the transistors are set to be $18\mu/1\mu$ and the RF input power is 14dBm [7]. The designed BGR consumes a static power of 61μW and generates an output reference voltage of 1.16V with a deviation of 1mV at 300kHz. The PSRR of this BGR as a function of frequency is shown in Fig. 9. The PSRR achieves more than -85dB below 10kHz while reducing to -60dB at 100kHz.

The designed LDO consumes only 2μW static power and has a response time less than 100ns, providing a stable $1.4V$ for the front end sensor. In order to allow the maximum

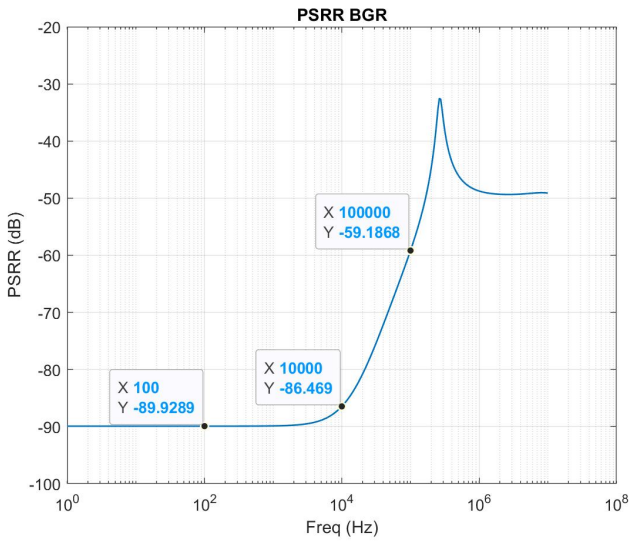

Fig. 9. Simulated PSRR of the BGR in this work. It achieves a PSRR of -59dB at 100kHz with a power consumption of 61 μW.

slew rate, the size of pass transistor in the LDO is set to be $4000\mu/180n$.

Table II compares this work to the state-of-the-art. This work consumes the least power.

TABLE II
COMPARISON WITH STATE-OF-THE-ART

Parameter		**This work**	[6]	[2]	[14]
Year		**2020**	2019	2018	2018
Application		**LSK**	LSK	LSK	LSK
Tech	nm	**180**	PCB	180	350
RF frequency	Hz	**433M**	1.93M	13.56M	433M
Supply-V	V	**1.4V**	3.5-4	2-3	1.5
Core-A	mm^2	**9**	28	25	2.1
Power Dissipation	W	**87μW**	44m	3.12m	92μ

V. CONCLUSION

This work demonstrates a low power wireless power management for system-on-chip sensors. Its small size and low power consumption allows it to be applied to various potential applications for remote powering. With a LSK circuit, the data generated by the sensor can be easily recovered at the primary side coil. A novel self-tuned LDO circuit is proposed to enhance the slew rate. The overall PMU budget is estimated to be 87μW and can be further improved by reducing the power of BGR if the PSRR constraints of BGR is not very demanding. The RF power is transmitted at 433MHz for a maximum transmission efficiency and the potential back-telemetry data rate can achieve up to 1MHz.

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