# Body Dust: A Wireless Electrochemical Sensor for In-vivo Glucose and pH Monitoring

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# Abstract

This research demonstrates an electrochemical sensor system for in-vivo glucose and pH monitoring based on wireless power and data transfer technique. The system consists of three blocks: inductive coils, power and data management, and front end sensor. The inductive coils are designed and fabricated with a size of $3mm*3mm$ by Dr Peilong [1], and the maximum power transmission efficiency is 19.2% at an RF frequency $433MHz$. Power and data management converts the receiving RF power to a stable $1.4V$ supply through a schottky rectifier, a band gap reference with a high power supply rejection ratio of $-60dB$ at $100KHz$ and a self tuned low drop out circuit with a fast response time of $100ns$. All these blocks are analysed and optimised in this work. The front end sensor detects pH information using an ISFET and an ion-selective electrode, and converts the current and voltage signal into frequency concurrently. The current input range is $80pA - 50nA$ and the output frequency range is from $210Hz$ to $300KHz$, while the voltage input achieves a range of $0V - 1V$ with an output frequency from $9.01Hz$ to $1.36HZ$. The frequency data is transmitted back to the primary coil using a load shift keying by controlling the parallel capacitor of the second side coil. The power consumption of the front end sensor system reduced to $11\mu W$, delivered by the data power management. The system layout is presented in this work, and the post-layout simulation works successfully.

A publication work is extracted from this work and attached in Appendix B, and will be submitted to the IEEE conference ISCAS 2021.

# Acknowledgment

First of all, I want to express my sincere gratitude to my supervisor Dr Pantelis Georgiou. You offered me a great chance to choose this topic for my final year project.

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Last but not least, I would like to sincerely thank my parents for being with me during this special and difficult time. Due to the Covid-19, most of the time I stayed at home alone. But your company on video calls always make me feels supported and motives me to keep going.

# Contents

# List of Figures

# List of Tables

# Abbreviations

**ASK:** Amplitude Shift Keying

**BGR:** Band Gap Reference

**BJT:** Bipolar Junction Transistor

**BPSK:** Binary Phase Shift Keying

**CTAT:** Complementary To Absolute Temperature

**Dapper:** Dual Amperometric and Potentiometric Power Efficient Sensor

**FSK:** Frequency Shift Keying

**ISFET:** Ion-Sensitive Field-Effect Transistor

**LDO:** Low Drop Circuit

**LSK:** Load Shift Keying

**NFC:** Near Field Communication

**PCE:** Power Conversion Efficiency

**POR:** Power On Reset

**PSK:** Phase Shift Keying

**PSRR:** Power Supply Rejection Ratio

**PTAT:** Proportional To Absolute Temperature

**PTE:** Power Transmission Efficiency

**RFID:** Radio Frequency Identification

**WPDT:** Wireless Power and Data Transmission

# Chapter 1

# Introduction

## 1.1 Motivation

GIVEN the interest in wireless power transfer (WPT) technology over the past decades, many areas have been further developed. Besides some traditional applications such as cellular phone, laptop and electronic vehicles, biomedical devices also benefit from building a wireless connection between humans' body and external circuits [6]. Power transfer from an out-body circuit to the in-body system is the pre-requisite for implanted devices, thus the demands for recharging battery and replacing the implanted component, no longer exist. As a result, no invasive battery wires are needed and the small volume battery does not limit the lifetime of the applications.

Amongst all the biomedical devices, growth and advances of electrochemical sensing have fulfilled and progressively elevated several areas for its sensitivities to specific analytes and the possibility of real-time biofluids sensing [7]. Among these analytes, one kind of important biomolecules used for medical purpose is glucose. However, glucose detection is potentially challenged by environment variability, such as biofluids pH. The detection of targeted biomolecules is consequently acquired by calibration of environment fluid pH. Thus, real-time and concurrent amperometric and potentiometric detection is necessary for these two different analytes.

Based on the above background, this project presents a low power implanted wire-

less electrochemical sensor for In-vivo glucose and pH monitoring system, using a dual amperometric and potentiometric power-efficient (Dapper) front end sensor [7]. The data detected by the sensor is transferred wirelessly through the inductive coils using load shift keying (LSK) scheme. However, the LSK will also cause the voltage ripple at the second side coil, thus affecting the voltage supply for the front end sensor. To mitigate this voltage fluctuation, a novel autonomous self-tuned LDO is proposed. For the purpose of low power consumption and simple structure, a Power On Reset (POR) circuit is utilised instead of any upload controlling circuit. The front-end dapper sensor consumes $11\mu W$ at a $1.4V$ supply and has a $0V - 1V$ potentiometry and $80pA - 1\mu A$ amperometry range [7]. The output frequency is up to $300kHz$ at the maximum input sensing current. The entire body dust system consumes $100\mu W$ power.

## 1.2 Outline

The report is organized as follows: Chapter 2 introduces the background of wireless power and data transfer (WPDT) system for the past few decades and presents the latest state-of-the-art technique. Then the principle of power transmission and data transmission are discussed along with the front end electrochemical sensing approach. The system architecture overview is given in Chapter 3, including the system's specification and objectives. Chapter 4 and 5 explain the power and data transmission circuit block in detail respectively, including theory, state-of-the-art work, circuit design, simulation and layout in cadence. Chapter 6 gives the system level simulation and layout, and discusses the test point consideration. The conclusion and future work are shown in Chapter 7.

# Chapter 2

# Wireless Power and Data Transmission System

THIS chapter represents the background of biomedical devices and its challenge, and illustrates why the Wireless Power and Data Transfer system is important to implanted biomedical devices. Important state-of-the-art designs are reviewed in this chapter. The last section talks about different front end sensor technique and introduces the proposed dual amperometric and potentiometric sensor.

## 2.1 Background

A biomedical device is any device designed for medical purposes, including prevention, diagnosis, treatment and rehabilitation [8]. These devices play a significant role in medical treatment such as diagnosing, monitoring patients health condition and providing prosthetic. The definition of biomedical devices is very general. Different varieties of products with different functions, from simple contact lenses and pH test paper to ventilator and medical robots, can be treated as biomedical devices.

The major factors driving the growth of this biomedical devices commercial market are the increasing public health awareness and a rising ageing population. The demands for high-quality, low-cost and reliable biomedical devices dramatically increase these years,

driving the growth of the global biomedical device industry. A research group predicts that the global biomedical market is forecast to reach $432.6 million by the year 2025, with a market growth of 4.1% compound annual growth rate each year [9]. The united states (USA), German and Japan are three leading countries in the biomedical device industry, providing the most advanced products and share the most markets globally. It is reported that the national health expenditures in the USA in 2015 had reached $3200 billion, accounting for around 10% of the USA GDP, while the biomedical industry also contributed 11.9% to its GDP in 2012. Biomedical device industry also expands fast in some developing countries such as China, with an average annual growth rate of 20% in the last ten years [9].

With the technology developing, biomedical devices are miniature, wearable and implantable. If a medical treatment device can be implanted inside a patient's body safely, it can improve the convenience of medical treatment and optimise patients experience without being constrained in the hospital. To date, most implanted devices are powered by batteries via wires. This introduces the necessity of invasive surgery and may cause skin infections, patient's discomfort and even the patient's health risk. Besides, these implanted batteries only contain fixed energy with limited capacity, which requires more invasive surgery to replace the battery. As a result, scientists have developed a wide range of method to make implanted devices harvesting energy possible, including infrared radiant energy, thermal energy, kinetic energy and wireless transfer energy.

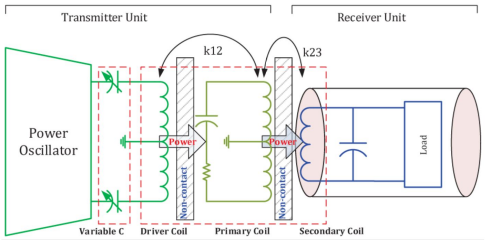
Among all these technologies, wireless transfer energy is the most commonly used and reliable technology. The development of a reliable low-cost wireless technology significantly boosts the biomedical industry over the decades. This technology replaces the clumsy wires and improves patient mobility. It also increases medical treatment efficiency by allowing medical equipment to be controlled remotely [10]. In this report, a wireless power transfer system, with wireless data transferring as well, is designed and manufactured.

## 2.2 State-of-the-art WPDT System

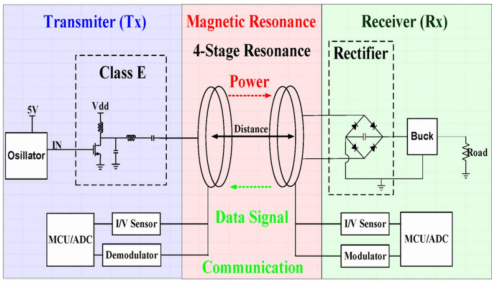
The interest in wireless transfer technologies, including near field communication (NFC), radio frequency identification (RFID), and wireless power and data transfer (WPDT), has increased over these years. NFC works as an observation of the near field magnetic field via inductive coupling between coils [11]. RFID technology can be found in many applications like access control and location. WPDT systems are commonly used in various mobile devices and medical sensors. Also, they are the most suitable technique for implanted biomedical sensors because the power and data can be transmitted remotely without causing harmful effects to the human body.

In the year 1865, Maxwell introduced the Maxwell's equation, which predicts the existence of the electromagnetic wave [12]. 2 years later, Hertz carried out the first WPT experiment, verifying the existence of electromagnetic wave [13]. After over a hundred years with the great effort and achievements from scientists and companies, WPDT is mature and plays an important role in biomedical sensors. The most popular mechanisms for transmitting power and data wirelessly are inductive coupling and magnetic resonance [11]. The power transmission efficiency (PTE) is the most important parameter in WPDT systems. In order to achieve an maximum PTE, Wen H. Ko proposed an inductance tapping and voltage doubling circuits [14], S. Maeda applied ferrite cores [15] and Roland Kadefors used efficient rectifying circuits [16].

With the help of previews research work, many research groups successfully developed advanced WPDT biomedical sensor systems. Furthermore, some research groups also analyse the performance of inductive links over tissues comprehensively [17]. Hongchang Zheng proposed a bidirectional communication WPDT system with power transferred in a range of 20 $kHz$ to 100 $kHz$ and data transferred at 10 $MHz$. The wireless gap achieves a distance of 10 $mm$ with a delivered power of 30 $W$ [18]. Heng-Ming Hsu leads a group which successfully developed a WPDT system operating at 6.78 $MHz$ for AirFuel specification. They achieve a PTE of 35% with a coil distance of 6 $cm$ [19]. A research group in the USA introduced a novel multi-coil coupled efficiency enhanced power link for WPDT systems, achieving a transfer gain 42 $dB$ higher than that of the two coil inductive




(a) System Block Diagram proposed by Heng-Ming Hsu, which achieves a PTE of 35% with a distance of 6 *cm* system [19].




(b) System Block Diagram proposed by Ruikuan using a multi-coil coupled technique [20].

Figure 2.1: Two block diagram of the state-of-the-art WPDT system

structure [20]. Many other research groups also successfully implemented WPDT systems, summarized in Table 2.1.

Table 2.1: SYSTEM CHARACTERISTICS AND COMPARISON WITH STATE-OF-THE-ART

| Parameter | Unit | [21] | [6] | [7] | [22] | [23] | [24] |
|---|---|---|---|---|---|---|---|
| Year | | 2019 | 2018 | 2018 | 2017 | 2016 | 2014 |
| Application | | LSK | LSK | LSK | ASK | FSK/UWB | OOK |
| Tech | $nm$ | PCB | 180 | 350 | 130 | 130 | 180 |
| RF frequency | $Hz$ | 1.93M | 13.56M | 433M | 1.5M | 916M | 13.56M /400M |
| Supply-V | $V$ | 3.5-4 | 2-3 | 1.5 | 2.5/3.3 | 2.5/3.3 | 1.8 |
| Core-A | $mm^2$ | 28 | 25 | 2.1 | 6 | 15.84 | 13.47 |
| Data Bandwidth | $Hz$ | 10k | 211k | 825 | 36M | 1.2M | 401M |
| INR | $\mu V$ | N.A | 2.09 | 1.8 | 1.13 | 7.5/4.2 | 1.77 |
| Power Dissipation | $W$ | 44m | 3.12m | $92\mu$ | 6.51m | 9.11m | 2.8m |

## 2.3 State-of-the-art Front End Sensor

The front end sensor is also a crucial block is body dust system. Among all the front end sensors, the most common use technologies are electrochemical, Piezoelectric and Thermal and Optical. Electrochemical sensors are commonly used in the biomedical sensing, and potentiometry and amperometry are the two most popular mechanisms. With the help of ion-selective electrode and its sensitivity to ions such as potassium and PH, electrochemical potentiometric sensing becomes much easier [25]. A new CMOS-based ISFET array

also proves its ability to determine the surrounding pH value and make amperometry possible [26]. However, the challenge also exits. The detection from the surrounding biofluid or other body environments may be interfered by other molecules and the concentration of these molecules also affects the performance of the electrochemical sensing. As a result, a real-time calibration is required for accurate sensing, and concurrent amperometry and potentiometry sensing becomes necessary [27]. Few research groups proposed some concurrent sensing systems. Sun [28] introduced a system that can switch between potentiometry mode and amperometry mode. In this report, a novel dual amperometric and potentiometric concurrent sensing front end is proposed [28].

# Chapter 3

# Wireless Power and Data Transmission System

## 3.1 System Architecture Overview

THE Figure 3.1 presents the block diagram of the integrated body dust system. The system is composed of two parts, external circuit, which is responsible for providing the RF energy and accepting the data information, and the internal circuit which is responsible for receiving and regulating the power and collect data. The inductive links were designed and manufactured [1] at an RF frequency $433MHz$ with a maximum PTE of 19.2%, allowing sufficient bandwidth for future multiple channel systems. The second side coil receives RF power from the primary coil and feeds this AC power to a rectifier. Then the AC signal will be converted to a DC signal through this rectifier, providing a stable voltage supply for the internal circuit with the help of a smoothing capacitor. A high power supply rejection ratio (PSRR) Band Gap Reference (BGR), following the rectifier, regulates the voltage supply to a stable 1.2V reference. At the last stage, a proposed self-tuned low drop out (LDO) circuit provides a stable 1.4V supply for the Dual amperometry and potentiometry power efficient sensor (Dapper) system. Based on the function of each block, the system can be divided into three blocks: inductive coil, data and power management, and Dapper sensor.

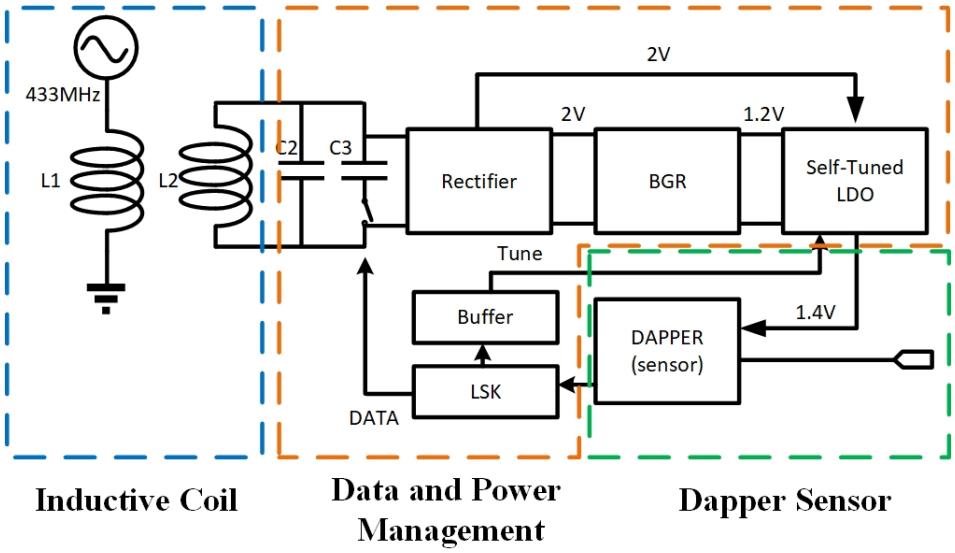



Figure 3.1: Body dust system architecture.

### 3.1.1 Inductive Coil

The inductive coil is the fundamental component in the WPDT system, and Figure 3.2 shows the classical structure of an inductive coil. Achieving a maximum PTE of inductive coil is the key design objective since the PTE of the coil normally limits the whole system's PTE performance. There are different methods to estimate the PTE of an inductive coil, and the reflected load model is used in this report.

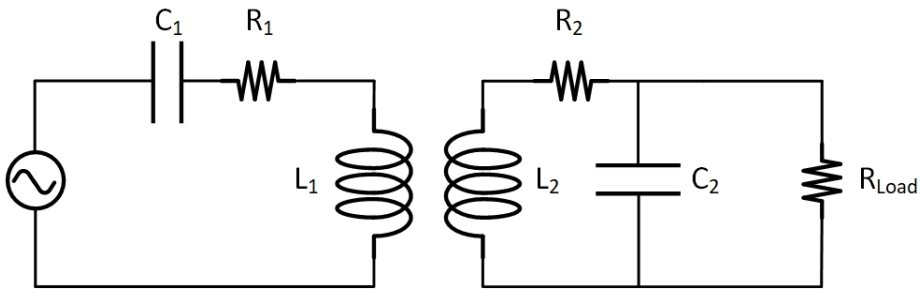



Figure 3.2: A conventional Inductive coil circuit.

The reflected model works at the resonant frequency, shown in the equation 3.1:

$$\omega = 2\pi f = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} \tag{3.1}$$

where $\omega$ is the resonant frequency, $L_1$, $C_1$ are the inductance and the capacitance of the primary coil, and $L_2$, $C_2$ are the inductance and the capacitance of the second coil. At the resonant frequency, it is assumed that all the capacitance and inductance are cancelled with each other, the reflected model becomes a resistor divider and the PTE achieves its maximum value [1], shown in the Figure 3.3.

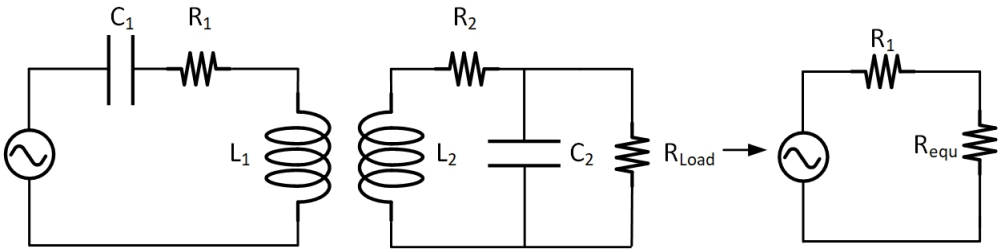



Figure 3.3: The simplification of the inductive coil circuit.

The quality factor Q of inductor $L_1$ and $L_2$ at both side of the coil are expressed as

$$Q_1 = \frac{\omega L_1}{R_1} \tag{3.2}$$

$$Q_2 = \frac{\omega L_2}{R_2} \tag{3.3}$$

The load Q factor at the secondary side is expressed as

$$Q_{2L} = \frac{Q_2 Q_L}{Q_2 + Q_L} \tag{3.4}$$

where $Q_L$ is the quality factor of the Load. At the resonant frequency, the circuit is simplified as a resistive divider and $R_{equ}$ can be written as

$$R_{equ} = k_{12}^2 \omega L_1 Q_{2L} \tag{3.5}$$

PTE can be calculated as

$$PTE = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I^2 * R_{\text{equ}} * \frac{R_{\text{Load}}}{R_2 + R_{\text{Load}}}}{I^2 * (R_{equ} + R_1)} \tag{3.6}$$

$$= \frac{R_{equ}}{R_{equ} + R_1} = \frac{k_{12}^2 \omega L_1 Q_{2L}}{k_{12}^2 \omega L_1 Q_{2L} + R_1} \frac{R_{\text{Load}}}{R_2 + R_{\text{Load}}} \tag{3.7}$$

$$= \frac{k_{12}^2 Q_1 Q_{2L}}{k_{12}^2 Q_1 Q_{2L} + 1} \frac{Q_2}{Q_2 + Q_{\text{Load}}} \tag{3.8}$$

where $Q_2$ and $Q_{Load}$ are the quality factor of the $R_2$ and $R_{Load}$, shown in the Figure 3.3. The maximum PTE is dominantly decided by $k_{12}$, represented as

$$k_{12} = \frac{M_{12}}{\sqrt{L_1 L_2}} \tag{3.9}$$

In this report, the inductive coil was manufactured by Dr Peilong Feng [1], operating at $433MHz$ to achieve the maximum PTE of 19.2% and the minimum power distribution within the Specific Absorption Rate constraint.

### 3.1.2 Data and Power Management

The key block in this WPDT system is the data and power management, receiving the power and modulating the data, shown in the Figure 3.4.

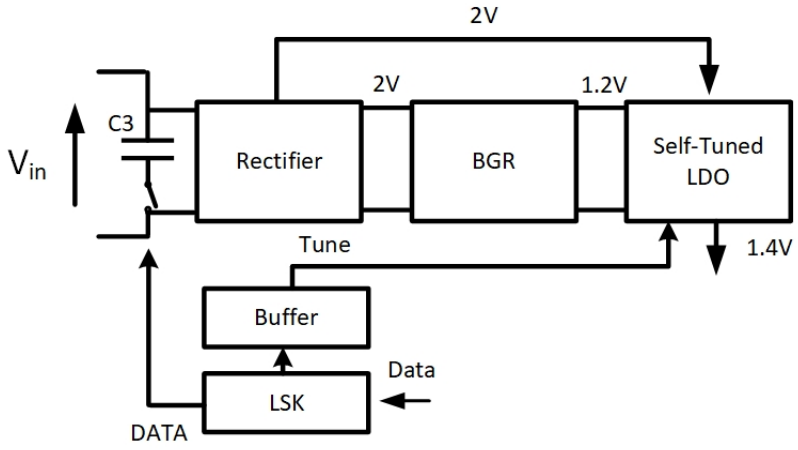



Figure 3.4: Data and power management block.

This block converts the RF energy from the external circuit and regulates the receiving signal through a rectifier, BGR and LDO to a stable 1.4 voltage supply for the front end sensor. A load shift keying (LSK) can change the impedance of the coil load responding to the digital data feeding to itself, thus the data can be transferred back to the external circuit wirelessly and simultaneously. But it also introduces a challenge to the WPDT system: the receiving voltage at the second side coil will also fluctuate once the LSK is operating, leading to a voltage ripple at the rectifier's output at a frequency same as the digitised data. So a high PSRR Band Gap Reference (BGR) is required to get rid of this ripple and ensure the power supply is stable regardless of the LSK. A novel self-tuned LDO is proposed at the last stage of the system to maintain the minimum power consumption.

### 3.1.3 Dual Amperometric and Potentiometric Power Efficient Sensor

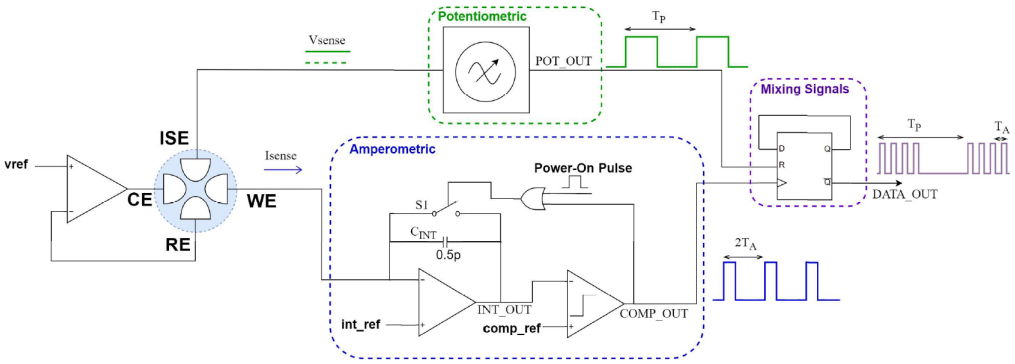



Figure 3.5: Front end sensor system architecture [2].

The front end sensor system includes a sensing circuit, an amperometric circuit, a potentiometric circuit and a D-Flip flop, shown in the Figure 3.5. The sensing circuit consists of four electrodes: a working electrode, a reference electrode, a counter electrode and an ion-selective electrode, and it can determine the surrounding environment pH and Glucose value to a current and a voltage signal concurrently. The potentiometric circuit is fundamentally a voltage controlled oscillator, able to convert a voltage signal to a square wave with a certain frequency. The amperometric circuit is made of a capacitor integrator

and a comparator, turning the input current into a digitised square wave signal. A low power D flip flop manages to mix two different frequency square wave and sends the data out through an LSK.

**Power On Reset circuit**

To minimize the power consumption and simplify the overall system, a Power On Reset (POR) circuit is utilised instead of the conventional uplink control circuit. A POR circuit can detect the power applied to the system and generate a reset signal to ensure the entire system operate correctly.

## 3.2 Specification / Objective

This research aims to design a wireless electrochemical sensor for in-vivo Glucose and pH monitoring with minimum power consumption. The system is based on an around-CMOS $3mm^2 * 3mm^2$ coil made by Dr Peilong [1]. The design technique is TSMC180BCD and all the circuits are designed and simulated using Cadence V6. The first objective is to design a WPDT system able to deliver enough stable power and $1.4V$ supply voltage to the Dapper sensor. The second objective is to optimize the front end Dapper sensor designed by Mr Daryl Ma [2]. The specification of the system is shown in the Table 3.1.

Table 3.1: Design Specification for Body dust system

| Parameter | Unit |
|---|---|
| Around CMOS coil Dimension | $3mm^2 * 3mm^2$ |
| Operating Frequency | $433MHz$ |
| Power efficiency | 5% |
| Voltage output | $1.4V$ |
| Power delivered to Load | $> 10\mu W$ |
| Download Data Rate | $1Hz - 300KHz$ |
| Chip Area | $3mm^2 * 3mm^2$ |

# Chapter 4

# Power Transmission System Implementation

## 4.1 Coil Design

Three different receiver coils have been designed, fabricated and tested by Dr Peilong Feng [1]: around-CMOS coil, above-CMOS coil and in-CMOS coil, shown in the Figure 4.1 .

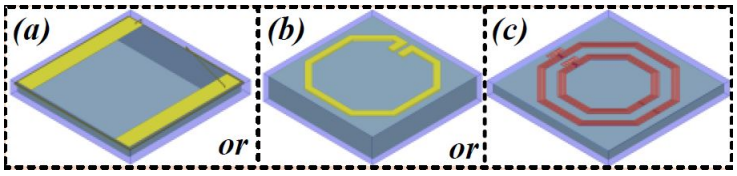



Figure 4.1: Diagram of three different coil designed by Dr. Peilong [1]. (a). around CMOS, (b) above-CMOS, (c) in-CMOS

The around-CMOS coil is made of $25\mu m$ diameter Au bond based on a $4mm$ square silicon substrate. The in-CMOS is fabricated using the standard CMOS technique made by aluminium metal layers. The above-CMOS has a simple structure compared to the other coils, which is fundamentally a thick metal layout on silicon. The performance of these three kinds of coils is compared in air and in tissue. The above-CMOS coil is chosen to be the receiving coil in this design because of its modest electromagnetic property and stability [1]. However, the mm-scale coil in biomedical applications still suffers from low

PTE. Thus a high PTE power modulating system is required.

## 4.2 Rectifier

### 4.2.1 Theory

MANY research works on the rectifier for WPDT systems have been published over the decades. Based on rectifier's topology, they can be divided into two groups: single-ended topology and differential topology [3], shown in Figure 4.2. Based on the conduction ability, rectifiers can be categorized into half-wave and full-wave rectifier, shown in the Figure 4.3.

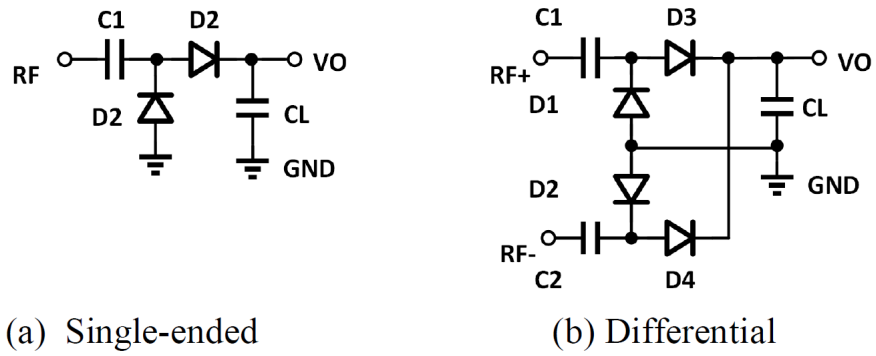



Figure 4.2: Schematics of single ended and differential rectifier [3].

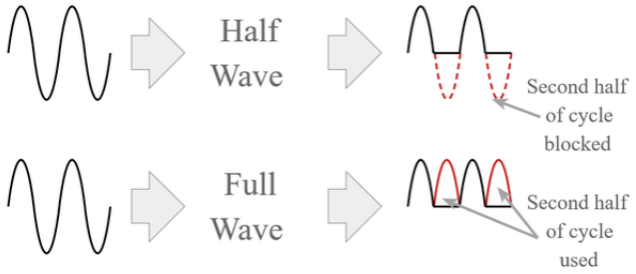



Figure 4.3: The wave output from halfwave rectifier and fullwave rectifier [3].

A half-wave rectifier with fewer diodes or transistors is preferred for low power and area-limited system since less voltage drop occurs across the components. However,

the power conversion efficiency (PCE) of halfwave rectifier is theoretically less than 50% because half of the input signal is blocked. The PCE of an idea halfwave rectifier is calculated as

$$\eta_{half} = \frac{(\frac{I_{max}}{\pi})^2 * R_L}{(\frac{I_{max}}{2})^2(r_f + R_L)} = \frac{\frac{4}{\pi^2}}{1 + \frac{r_f}{R_L}} \tag{4.1}$$

where $R_L$ is the load resistance and $r_f$ is the diode forward resistance. For $r_f \ll R_L$ ,

$$\eta_{half} = \frac{4}{\pi^2} = 40.6\% \tag{4.2}$$

The PCE of an idea fullwave rectifier is calculated as ($r_f \ll R_L$)

$$\eta_{full} = \frac{\frac{8}{\pi^2}}{1 + \frac{r_f}{R_L}} = 81.2\% \tag{4.3}$$

Its PCE is twice than that of a half wave rectifier. Thus fullwave rectifier is applied in this research.

### 4.2.2 State of the art

In CMOS technology, rectifiers are commonly implemented using diode-connected transistors due to cost and area consideration, but their PCE is worse than the conventional diode rectifiers. Several techniques have been proposed to enhance the CMOS-based rectifier PCE, such as Vth cancellation techniques [3] and active rectifiers [29]. A Vth cancellation technique aims to reduce the forward threshold voltage to increase the voltage conversion rate and reduce the power loss across the transistors. H. Nakamoto proposed a method using a capacitor to store the threshold voltage between the gate-source terminal of the transistors, shown in the figure [30]. However, for fully storing the required threshold voltage, a large capacitor is needed with a large area wasted.

A research group also proposed a new switch rectifier [29], replacing the diode-connected transistors with a pair of PMOS switches. It achieves a VCR of 87% and PCE of 71% at the input magnitude of $2.7V$. But it still suffers from a massive area occupancy due to two large capacitors. S. Saeid Hashemi [29] introduced a novel fully cross-coupled rectifier with bulk terminal regulation technique [31], shown in Figure 4.5.

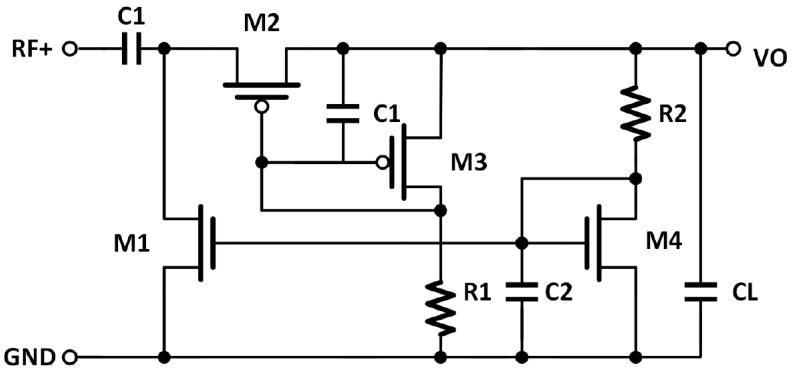
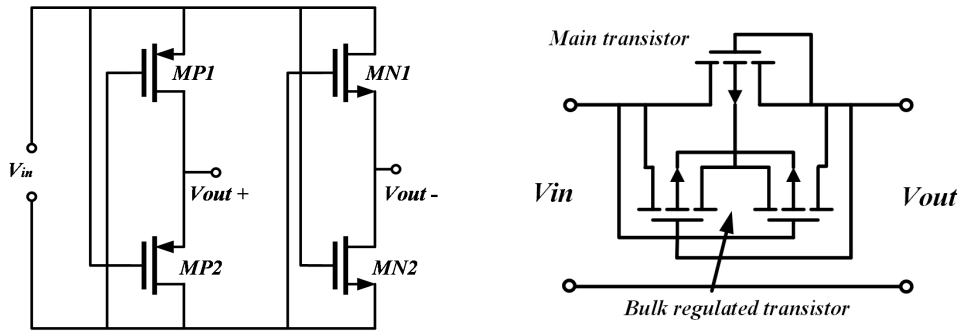



Figure 4.4: Schematic of a Vth cancellation rectifier.




(a) Fully cross-coupled rectifier (b) Bulk regulated transistors

Figure 4.5: The bulk regulated transistors are added to every transistors in fully cross-coupled rectifier, ensuring the main transistor's source terminal are always connected to the lowest potential

When the fully cross-coupled rectifier in the Figure 4.5 is operating, only one branch of the circuit turns on, either MN1 and MP2 or MP1 and MN2, forcing the output node Vout+ always higher than Vout-. The bulk regulated transistors shown in the Figure 4.5 ensures the main transistor's source terminal are always connected to the lowest potential, minimising the body effect. Thus the bulk regulated transistors have to be added to every transistor in fully cross-coupled rectifier [31]. The dropout voltage across the transistors can be kept minimum if the ratio of length and width is small enough, as shown in the 4.4

$$V_{\text{loss}} = V_n + V_p = \sqrt{\frac{2I_d L_n}{\mu C_{ox} W_n}} + \sqrt{\frac{2I_d L_p}{\mu C_{ox} W_p}} \approx 0.4V \tag{4.4}$$

Although this technique improves the voltage conversion ratio by reducing the voltage loss across the transistors, it suffers from low PTE due to the possibility of flow back current.

The simulation in cadence shows that it can only achieve a maximum PCE of 20% at RF frequency $433MHz$ with a load of $40K\Omega$.

### 4.2.3 Proposed Rectifier and Comparison

In order to find the best fit for our inductive coil and achieve a maximum VCR and PTE, different topology of rectifiers are simulated and compared using TSMC180 technology kit, shown in the Figure 4.6. All the transistors size are set to be $20\mu m/350nm$ to have a fair comparison. Different size of smoothing capacitors are placed to have a similar stable output voltage. The performance is concluded in the Table 4.1.

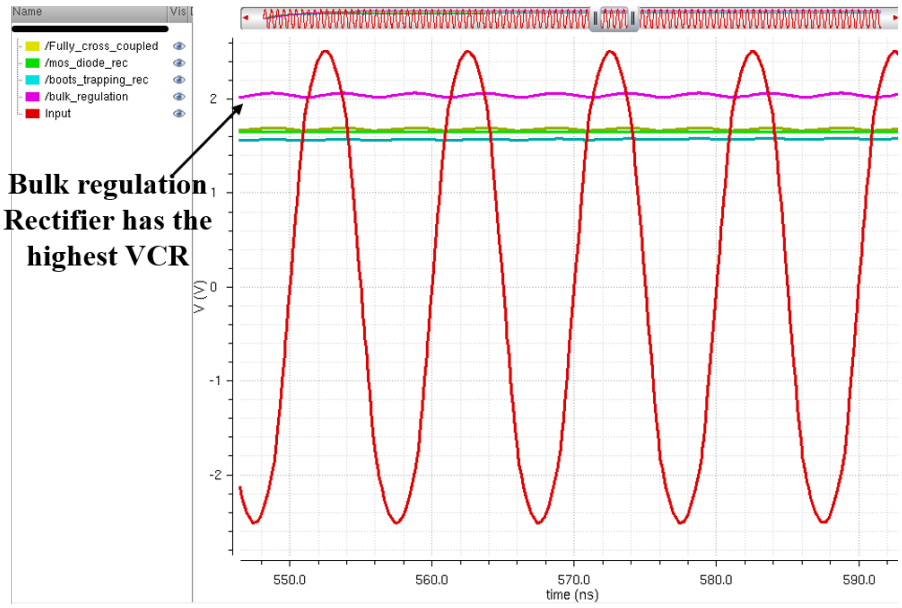



Figure 4.6: Waveforms of different topology of rectifiers.

Table 4.1: Performance metrics of different topology rectifiers

| Performance | Cross coupled | Diode-connected | Boots trapping | Bulk regulated |
|---|---|---|---|---|
| Vin (V) | 3 | 3 | 3 | 3 |
| Vout (V) | 1.73 | 1.60 | 1.4 | 2.156 |
| VCR | 57% | 53.4% | 46.7% | 71.87% |

However, the PTE of these CMOS based rectifiers is not desirable, less than 20% at $433MHz$. So eventually a conventional rectifier using the schottky diode, provided by TSMC180 technology, is applied, shown in the Figure 4.7.

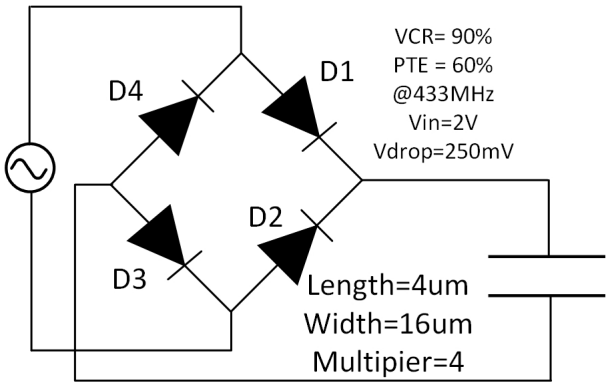



Figure 4.7: Shottky diode rectifier.

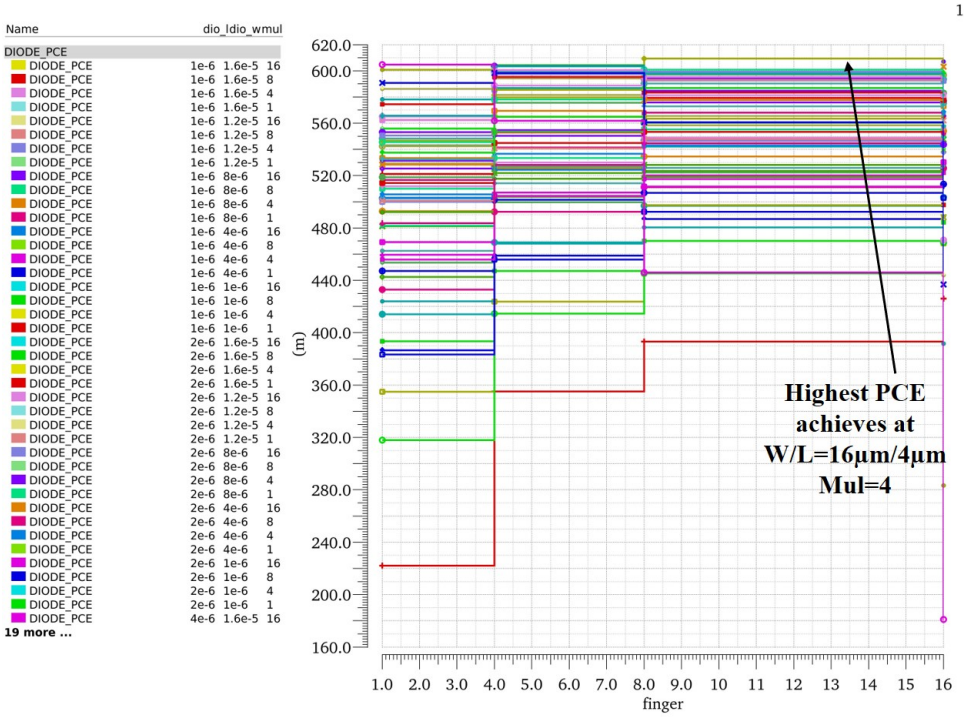



Figure 4.8: Different size of diodes are compared to achieve the highest PCE. The best fit is found at the W/L = $16\mu m/4\mu m$ and multipier=4.

In order to find the best performance of the rectifier, different size of diodes are tested, shown in the Figure 4.8. A large width to length radio means high current capacity but more power consumption. The Maximum PTE and VCR is achieved as the length of the diode is set to $4um$, width is $16um$ and multiplier is 4 at $V_{inpeak} = 2V$. The voltage loss across each diode is measured to be $250mV$. A smoothing capacitor is added after the

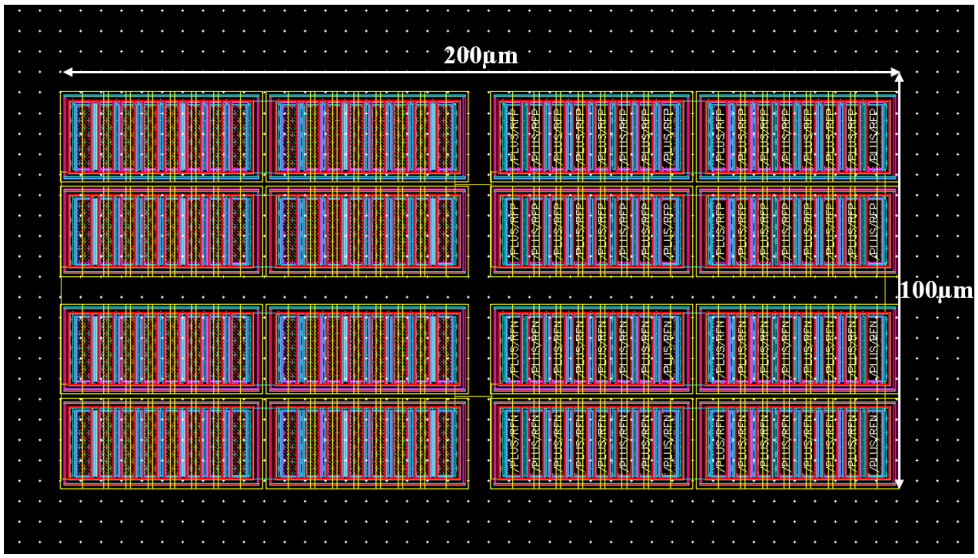



Figure 4.9: Shottky diode rectifier layout.

rectifier to stabilize the output voltage and reduce its ripple. An on-chip $300pF$ capacitor is applied for a balance between area and performance. Due to its simple structure, there is no Monte Carlo simulation deviation with 100 Monte-Carlo tests.

Figure 4.9 shows the layout of the rectifier. Thick tracks are required to connect these components since large current will pass through it. The parasitic resistance and capacitance are considered using post-layout simulation, and the waveform is shown in the Figure 4.10. The green line represents the output voltage of the rectifier without post-layout consideration while the red line represents the output voltage of the rectifier with post-layout consideration.

After considering the parasitic impedance and the track resistance, the output voltage of the rectifier is affected due to the increased impedance, decreasing from $2.4V$ to $2V$. Besides, the input voltage is also decreased due to the resonate frequency shift at the second side coil caused by the parasitic impedance.

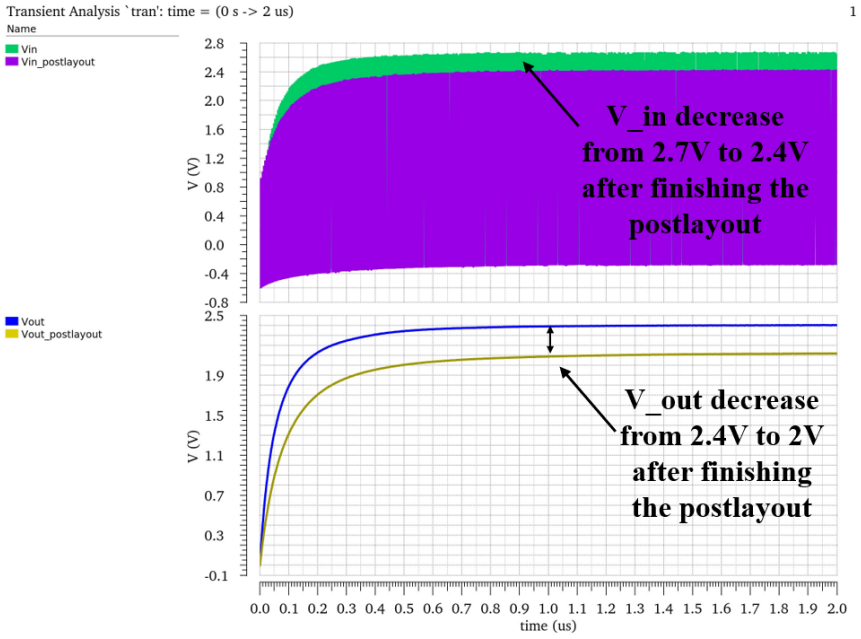



Figure 4.10: The simulation waveform of post-layout rectifier.

## 4.3 Band Gap Reference

### 4.3.1 Theory of BGR

The voltage reference is a fundamental component in every analogue and mix-mode circuit, providing a constant voltage level regardless of supply and temperature variation. The band gap reference is the most popular voltage reference first invented by R.J. Widlar in 1971 [32]. The first temperature-independent voltage reference is fulfilled by introducing a combination of a proportional to absolute temperature (PTAT) voltage, generated by two bipolar junction transistors (BJT) working at different current density, and a complementary to absolute temperature (CTAT) voltage, provided by a forward bias BJT junction. This technique successfully provides a voltage reference same as silicon bandgap voltage around 1.2V.

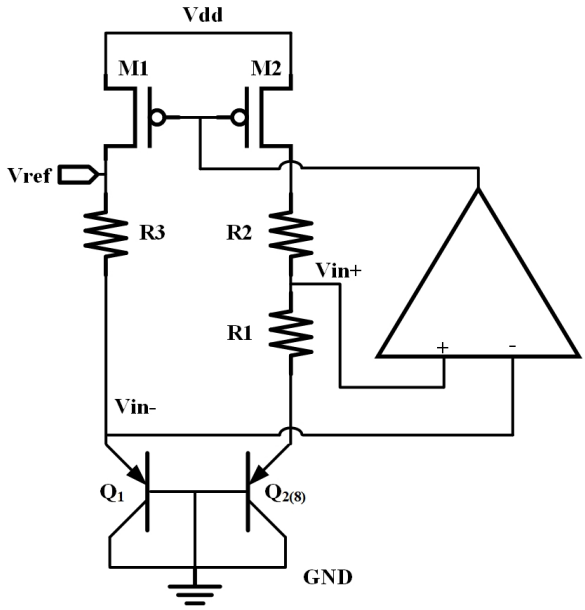



Figure 4.11: Schematic of a basic BGR.

Figure 4.11 shows the schematic of a basic band gap reference. This BGR consists of two BJT $Q_1$ and $Q_{2(8)}$, of which size is eight times bigger than that of $Q_1$, a current mirror pair M1 and M2, three resistance and an Opamp. The high gain Opamp ensures the nodes Vin+ and Vin- at the same potential. The PTAT voltage can be generated by $Q_1$ and $Q_{2(8)}$ which have different size but equal emitter current due to the current mirror, shown in 4.5.

$$I_{R1} = \frac{V_{be1} - V_{be2}}{R_1} = \frac{V_T \ln(8)}{R_1} \tag{4.5}$$

where $V_T$ is the thermal voltage, around $25mV$ at $25°C$. The CTAT voltage $V_{be1}$ is generated from a base-emitter junction of a BJT, which is fundamentally a forward PN junction, having a negative temperature dependent nature around $-1.5mV/°C$ [33]. After summing these two voltage, the reference voltage can be given by

$$V_{ref} = V_{be1} + I_{R1}R_3 = V_{be1} + \frac{R_3}{R_1}V_T \ln(8) \tag{4.6}$$

The temperature sensitivity can be calculated, given by:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{be1}}{\partial T}\bigg|_{T=T_r} + \frac{R_3}{R_1}\ln(8)\frac{\partial V_T}{\partial T}\bigg|_{T=T_r} \tag{4.7}$$

$$\frac{\partial V_{be1}}{\partial T} = -1.5mV/^\circ K \tag{4.8}$$

$$\frac{\partial V_T}{\partial T} = 0.087mV/^\circ C \tag{4.9}$$

For a minimum temperature dependence, $\frac{\partial V_{ref}}{\partial T}$ should be zero if $R_2$ and $R_3$ are set to be $100k\Omega$ and $R_1$ is set to be $10k\Omega$, and $V_{ref} = 1.2V$ .

$$\frac{\partial V_{ref}}{\partial T} = -1.5mV/^\circ K + \frac{R_3}{R_1}\ln(8) * 0.087mV/^\circ C \tag{4.10}$$

$$= \frac{\partial V_{ref}}{\partial T} = -1.5mV/^\circ K + \frac{100k}{10k}2.08 * 0.087mV/^\circ C \simeq 0 \tag{4.11}$$

### 4.3.2 State of The Art

In 1974, Paul invented the first commercial bandgap reference circuit, capable of providing $1.2V$ with a minimum supply voltage of $1.4V$. 30 years later, P.K.T. Mok [34] introduced a low voltage BGR, providing 0.6V reference with the help of an extra Opamp as its output buffer. Hongchin Lin [35] proposed a subthreshold BGR consuming only $2.4\mu W$ at a supply voltage of $1V$. This design has $1.3mV$ voltage variation from $-20^\circ C$ to $100^\circ C$. Recently, many research groups are devoted to designing low-power, small area and high accurate BGR. Wadhwaa designed a low-power high accurate bandgap reference using 16nm FinFet technique, achieving the maximum variation of $8mV$ at an output voltage of $0.605V$ [36]. Singh introduced a trimless and resistor-less BGR with a worst case accuracy up to $25ppm/^\circ C$ [37].

### 4.3.3 Challenge and Design Constraints

However, most of the BGR discussed in the last section suffers from low power supply rejection ability at a low power supply mode. Due to the existence of the LSK in this design, the voltage supply fluctuates from 2.05V to 2.1V at a frequency up to $300KHz$, same as

that of the digitized data from sensor. The performance of conventional BGR deteriorates, mainly because the PSRR of the low power Opamp decrease at a high frequency, and the output reference also ripples corresponding to the LSK, shown in the Figure 4.12.

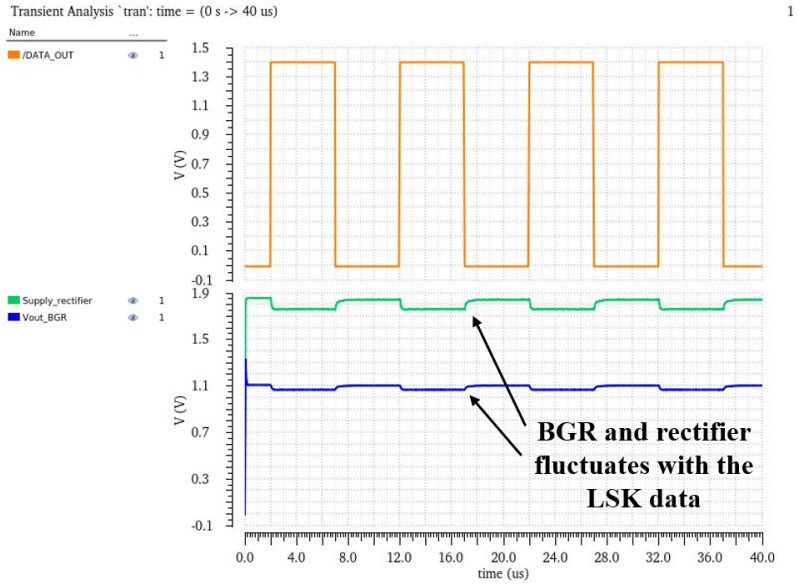



Figure 4.12: Voltage reference (blue line) is affected by the high frequency power supply.

### 4.3.4 Proposed High PSRR BGR

In order to analyse the PSRR of BGR and to design a high performance BGR, a small signal analysis model for the basic BGR in Figure 4.11, is used, shown in Figure 4.13.

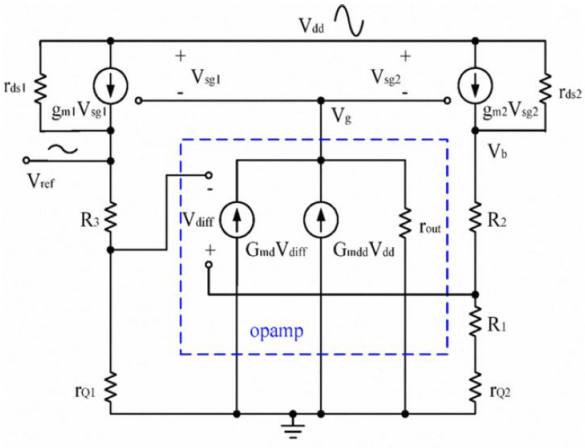



Figure 4.13: The small signal analysis model of conventional BGR [4].

The output resistance of the current pair transistors are ignored, under the assumption that they are long channel CMOS. The small signal analysis is shown below [4]:

$$\begin{aligned} v_g &= A\left(\beta_2 v_b - \beta_1 v_{ref}\right) + A_{dd} v_{dd} \\ g_{m1,2}\left(v_{dd} - v_g\right) r_{Q1} &= \beta_1 v_{ref} \\ g_{m1,2}\left(v_{dd} - v_g\right)\left(r_{Q2} + R_1\right) &= \beta_2 v_b \\ \beta_1 &= \tfrac{r_{Q1}}{r_{Q1}+R_3} \\ \beta_2 &= \tfrac{r_{Q2}+R_1}{r_{Q2}+R_1+R_2} \end{aligned} \tag{4.12}$$

where $A = v_g/v_{diff} = G_{md} r_{out}$ is the gain of Opamp, and $A_{dd} = v_g/v_{dd} = G_{mdd} r_{out}$ is the PSRR of Opamp. Thus the PSR of the BGR can be represented as :

$$\begin{aligned} \frac{v_{ref}}{v_{dd}} &= g_{m1,2}\left(r_{Q1} + R_3\right) \frac{1 - A_{dd}}{1 + g_{m1,2}\left(r_{Q2} + R_1\right) A - g_{m1,2} r_{Q1} A} \\ &\approx g_{m1,2}\left(r_{Q1} + R_3\right) \frac{1 - A_{dd}}{1 + g_{m1,2} R_1 A} \\ &\approx \left(\frac{r_{Q1} + R_3}{R_1}\right)\left(\frac{1 - A_{dd}}{A}\right) \end{aligned} \tag{4.13}$$

where $r_{Q1}$ is the on-resistance of the BJT $Q_1$, which is much smaller than $R_3$, and $\frac{r_{Q1}+R_3}{R_1} \simeq 10$. $\frac{v_{ref}}{v_{dd}}$ mainly depends on gain $A$ and PSRR of the Opamp $A_{dd}$. The smaller $\frac{v_{ref}}{v_{dd}}$ be, the higher the PSRR of BGR be. Having a higher open loop gain of Opamp may improve the PSRR at slow operation mode but deteriorate its performance at high frequency band. Thus a large gain band width product Opamp is desired but it consumes too much power, which is unacceptable in biomedical WPDT systems. It is also noticeable that if the PSRR of Opamp, $A_{dd}$, equals to 1, then the second term of $\frac{v_{ref}}{v_{dd}}$ becomes to 0, thus an infinite PSRR of BGR can be achieved. This can be explained that, if the Opamp can follow the fluctuation of power supply, the gate-source voltage $V_{gs}$ of current mirror transistors remains unchanged. With the assumption of long channel length of current mirror pair, the drain current will not be affected by the drain-source voltage $V_{ds}$, but remain constant regardless of power supply ripple. Thus the output voltage keeps constant, and a high PSRR BGR is realised.

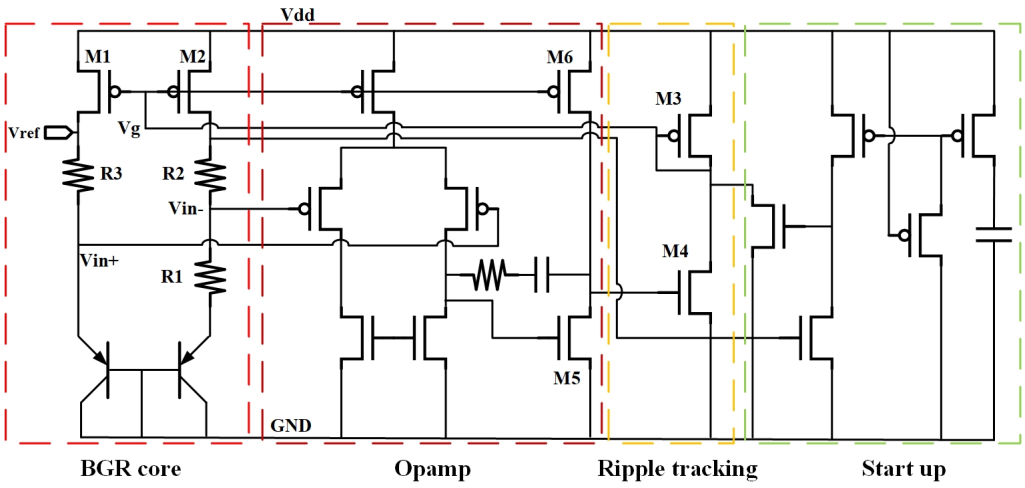



Figure 4.14: Schematic diagram of a high PSRR BGR .

Figure 4.14 shows the schematic diagram of a high PSRR BGR. This circuit consists of four blocks: bandgap core, Opamp, supply ripple tracking block and start up block. The bandgap core and Opamp are a conventional BGR structure providing a temperature-independent voltage reference. A supply ripple tracking block is added between the gate terminal of current mirror M1 and M2 in BGR core and the output of the Opamp. The key in this circuit is the diode-connected transistor M3. It has a low impedance of $\frac{1}{g_{m3}}$, and the PSRR at node $v_g$ is given by:

$$A_{dd} = \frac{v_g}{v_{dd}} = \frac{r_{ds4}}{1/g_{m3} + r_{ds4}} \approx 1 \tag{4.14}$$

As proved in 4.13, with a diode-connected M3, the supply ripple will be tracked at the node $V_g$, thus the $V_{gs}$ of current mirror M1 and M2 keeps constant as well as their drain current. A high PSRR BGR is eventually fulfilled. A start up circuit is attached to this circuit, enabling M1 and M2 working at the saturation region during the power on stage, reducing the settling time.

However, this ripple tracking block along with the two-stage Opamp forms a three-stage Opamp, deteriorating the stability of the overall circuit. Besides, the transistors M5, M4, M3, M6 form a local positive feedback, which may lock the circuit and shut it down. Thus, the second and third stage gain should be reduced to slow down this local positive

feedback, having the overall negative feedback work correctly. The size of differential pair is set to be $40\mu m/3\mu m$, M5 is set to be $30\mu m/3\mu m$, and M4 is set to be $6\mu m/7\mu m$.

### 4.3.5 Simulation and Layout

The simulation waveform of the proposed BGR is shown in the Figure 4.15. The orange line shows that a constant voltage reference is achieved regardless of a high frequency power supply ripple.

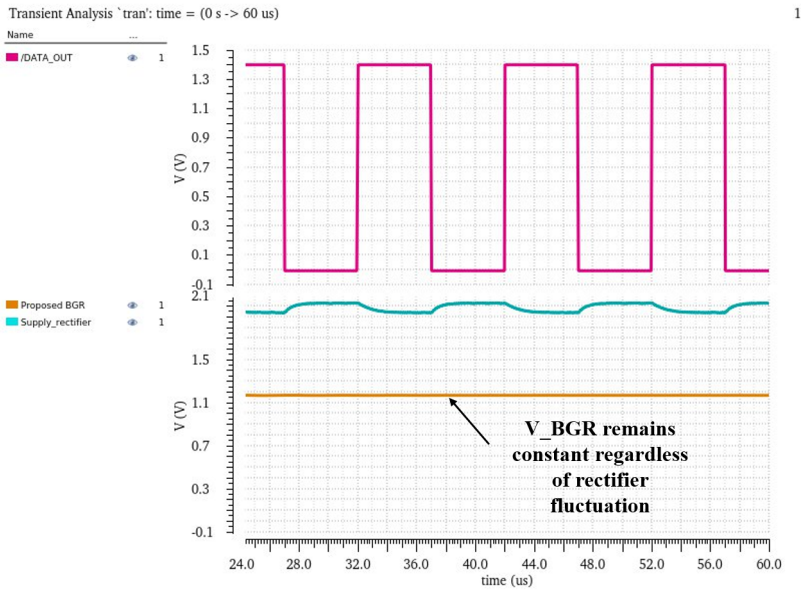



Figure 4.15: Waveform of the proposed high PSRR BGR .

Figure 4.16 and 4.17 shows the AC analysis and the PSRR of BGR as a function of frequency. The AC analysis shows the output ripple magnitude as a function of frequency when the input AC magnitude is set to be $100mV$. This proposed BGR achieves a PSRR of $-89dB$ at base band and $-59dB$ at $100KHz$.

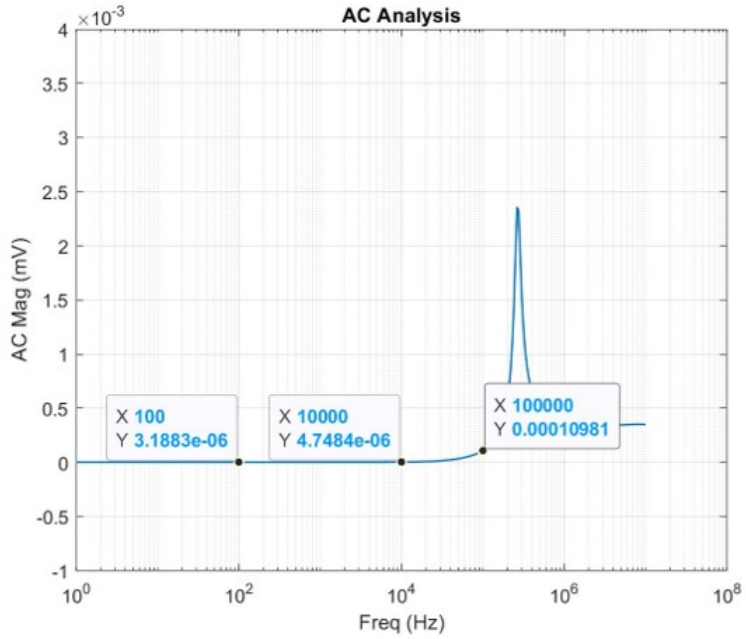



Figure 4.16: AC analysis of the proposed BGR.

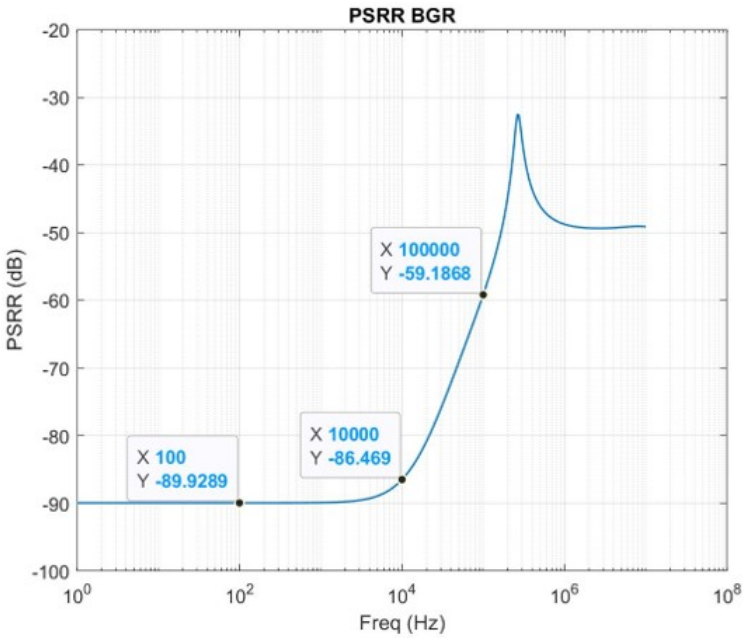



Figure 4.17: PSRR of the proposed BGR.

The layout of this BGR is shown in the Figure 4.18. A large area of capacitors are used to ensure the voltage reference is smooth.

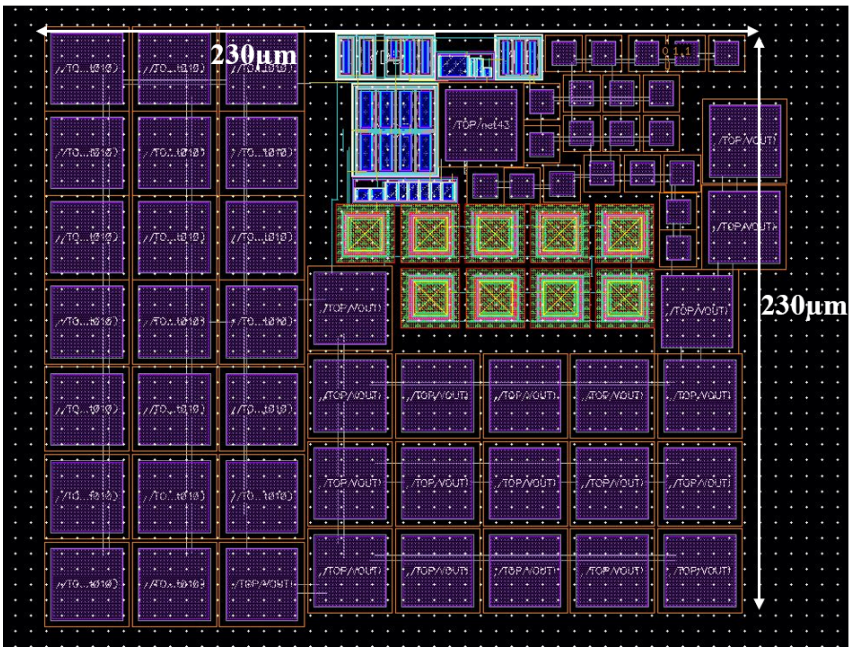



Figure 4.18: The diagram of layout the proposed BGR and a large area of capacitor is used to smooth the voltage reference.

This BGR has to be modified after post-layout simulation since all the wire resistance and parasitic capacitance should be considered. To achieve a high accurate voltage reference, the resistance value in BGR core should be accurate. So the resistance of R3 and R2 are set to decrease to $99.85K\Omega$ considering $150K\Omega$ wire resistance. The post-layout simulation is shown in the Figure 4.19. The output voltage reference increase from $1.15V$ to $1.17V$ after considering all the wire resistance and parasitic impedance.

The Monte Carlo simulation is shown in the Figure 4.20. All 100 runs successfully generate a voltage reference, ranging from $1.145V$ to $1.187V$

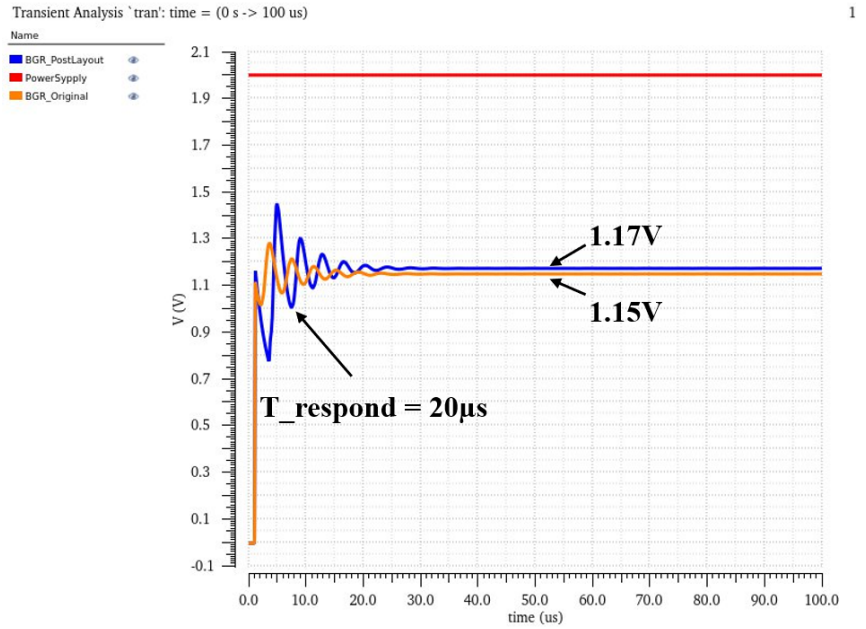



Figure 4.19: The comparison between the original BGR output and the post-layout BGR Oupout.

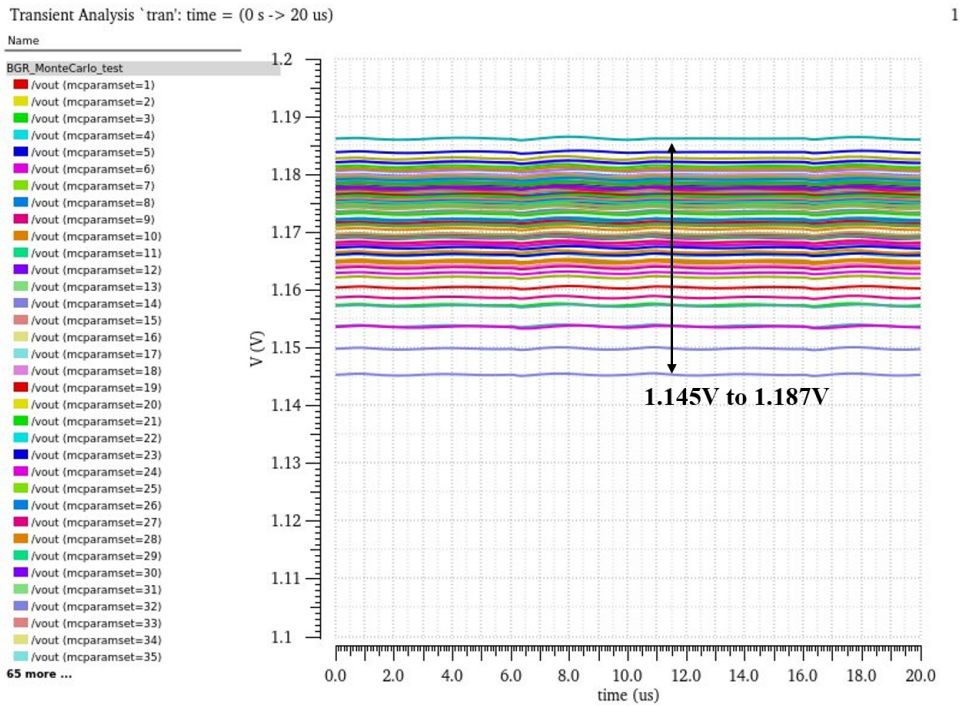



Figure 4.20: A MonteCarlo test of 100 runs of BGR.

## 4.4 Self-Tuned-LDO

### 4.4.1 Theory

Low dropout circuits are widely used in portable battery-powered and WPDT systems where the energy delivered is very limited, and it can convert the supply voltage to an accurate and low output voltage.

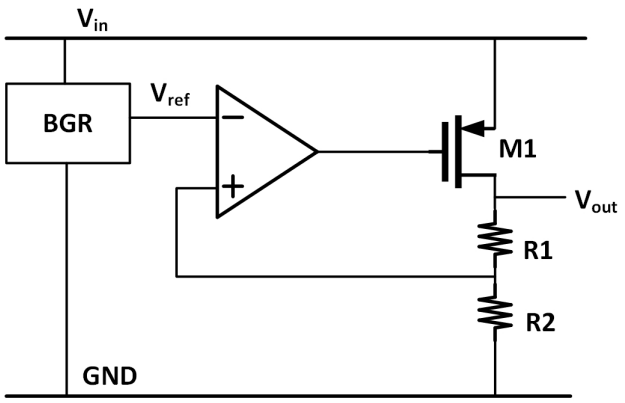



Figure 4.21: Schematic diagram of a conventional LDO.

Figure 4.21 shows the schematic of a conventional LDO circuit, including a voltage reference, an Opamp, two resistors and on PMOS transistor. The high gain Opamp, normally an error amplifier, forces its two input terminals at a same potential level. $R1$ and $R2$ are set such that $V_{out}$ can be $1.4V$. A large size PMOS M1 is required to allow large current passing through, thus increasing its slew rate and reducing responding time. However, the large size of M1 also introduces large gate capacitance, which deteriorates the high-frequency performance and slew rate [38], according to 4.15.

$$S_R = \frac{\partial V_{out}}{\partial t} = \frac{I_{out}}{C_g} \tag{4.15}$$

From Equation4.15, A large quiescent current can improve the slew rate as well, but it may consume more power. Both low power and high slew rate performance can not be fulfilled simultaneously by using the conventional circuit.

### 4.4.2 State of The Art

Over the decades, many works on high performance and low power LDO has been published. Hoi Lee introduced a current efficient analog driver for CMOS LDO, which achieved over 43 timers improvement in slew rate and settling time [38]. Other popular effective strategies are adaptive and dynamic biasing techniques [39]. Gabriel A. proposed a low quiescent current LDO using an extra small transistor in parallel with power transistor to sense the current. Once the current increment is detected, the bias current of power transistor increases adaptively and also the slew rate is improved. RC high pass filters are commonly used in dynamic biasing techniques [40]. The output voltage will be sensed by the High Pass Filter (HPF) and once there is a spike occurs, the biasing current of the Opamp will be boosted. But this requires a large area of capacitor to couple the voltage. Jianping Guo [39] invented a digital detecting technique LDO to replace the large capacitance which only consumes $3.9\mu A$ under static mode.

### 4.4.3 Proposed Self-tuned-LDO

#### Dynamic Bias Current LDO

Dynamic bias current LDO proves to be effective over these years [41]. Event detection can be operated at either an internal net or the output terminal.

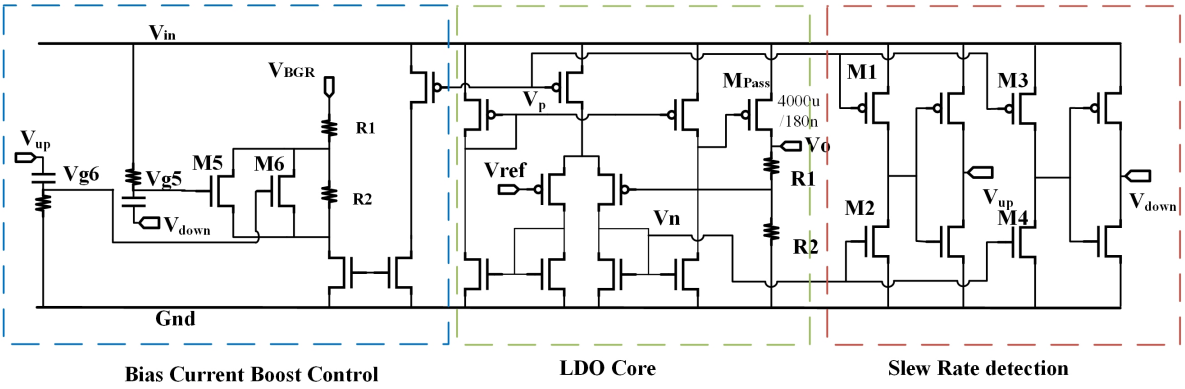



Figure 4.22: Schematic diagram of a dynamic bias current LDO. It consists of three blocks: a bias current boost control block, a LDO core and a slew rate detection

Figure 4.22 shows a schematic diagram of a dynamic bias current LDO introduced by Macro Ho [41]. It consists of three blocks: a bias current boost control block, an LDO core and a slew rate detection block. At the steady stage, the $V_P$ and $V_N$ are biased by the LDO core. $V_{up}$ is set to be high potential level and $V_{down}$ is near the ground at the specific W/L ratio of transistor M1, M2, M3 and M4 [41]. Because the NMOS M2 and M4 are connected with PMOS M1 and M3 in series respectively, their drain current are the same. If the aspect ratio W/L of PMOS M1 transistor is bigger than that of NMOS M2, the drain terminal of PMOS M1 (the drain terminal of NMOS M2), will be pushed to a higher voltage level to allow the same current to flow. Similarly, if the aspect ratio of W/L of NMOS M4 is bigger than that of PMOS M3, the drain terminal NMOS M4 will be pushed near the ground. In this design, the size of these transistors are: M1: $20\mu m/1\mu m$, M2: $30\mu m/1\mu m$, M3: $30\mu m/1\mu m$, M4: $20\mu m/1\mu m$. This setup will allow more swing range to trigger the bias current boost control circuit.

The Bias-current-boost control block is fundamentally a high pass filter switch. Once the slew rate detection operates, $V_{up}$ or $V_{down}$, the output of an inverter, will flip. This pulse will feed to an RC HPF, then triggers M5 or M6 to switch on. The large value resistance R2 then will be shorted and the bias current will boost, depending on a small resistance R1. The time constant $\tau$ will decide the time that it takes to have $V_{g5}$ and $V_{g6}$ decay back to the steady state. Thus, the RC HPF provides automatic switch-off function, further increasing the power efficiency.

However, this dynamic LDO needs the input supply voltage to change big enough so that the internal node fluctuation can be detected. In our system, the $V_{in}$ fluctuation has been reduced to $50mV$. Once the LSK operates and the $V_{in}$ changes, the internal node $V_p$ and $V_n$ fluctuates. But the fluctuation magnitude in our work is not big enough to trigger the inverter. Thus the bias boost circuit will not work, shown in the Figure 4.23.

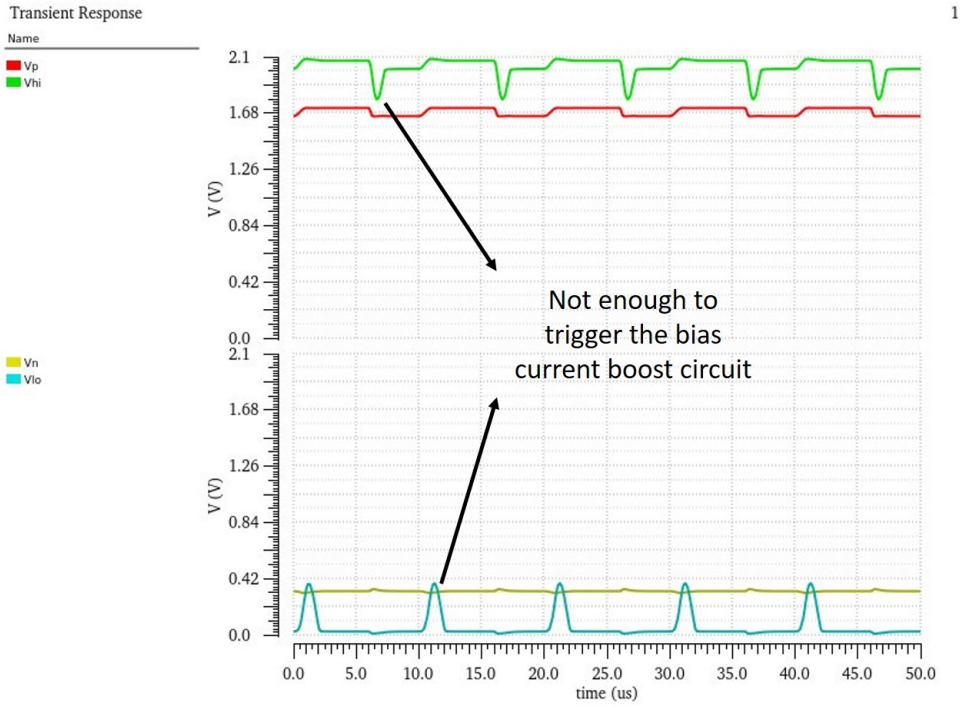



Figure 4.23: Waveform of a dynamic bias current LDO, the internal detection node is not strong enough to trigger the bias current boost circuit

### Self-Tuned LDO

The improved self-tuned LDO circuit is proposed in this section, shown in the Figure 4.24.

In this circuit, the proposed LDO consists of two blocks: LDO core and a self-tuned controller. There is no slewing detection circuit in this system since the bias current boost is controlled by the Data, the same signal controlling the LSK. As a system design level, the Dapper sensor data can also be used by this LDO. Thus the $V_{in}$ fluctuation and bias current boost can take place simultaneously. The two switches are implemented using NMOS because it is easier to turn on from a low potential voltage. The inverter buffers are added after the RC HPF to switch on the NMOS strongly. The steady stage bias current is $300pA$, increasing to $100\mu A$ once the boost circuit works.

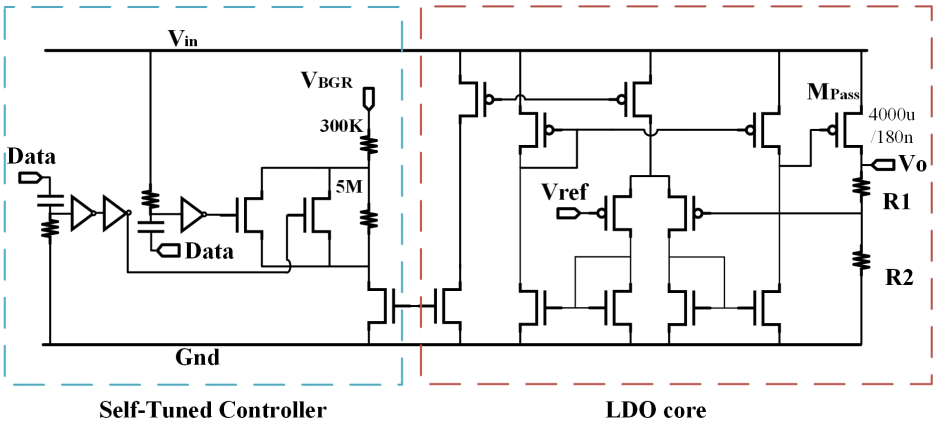



Figure 4.24: Schematic diagram of the proposed self-tuned LDO.

### 4.4.4 Simulation and Layout

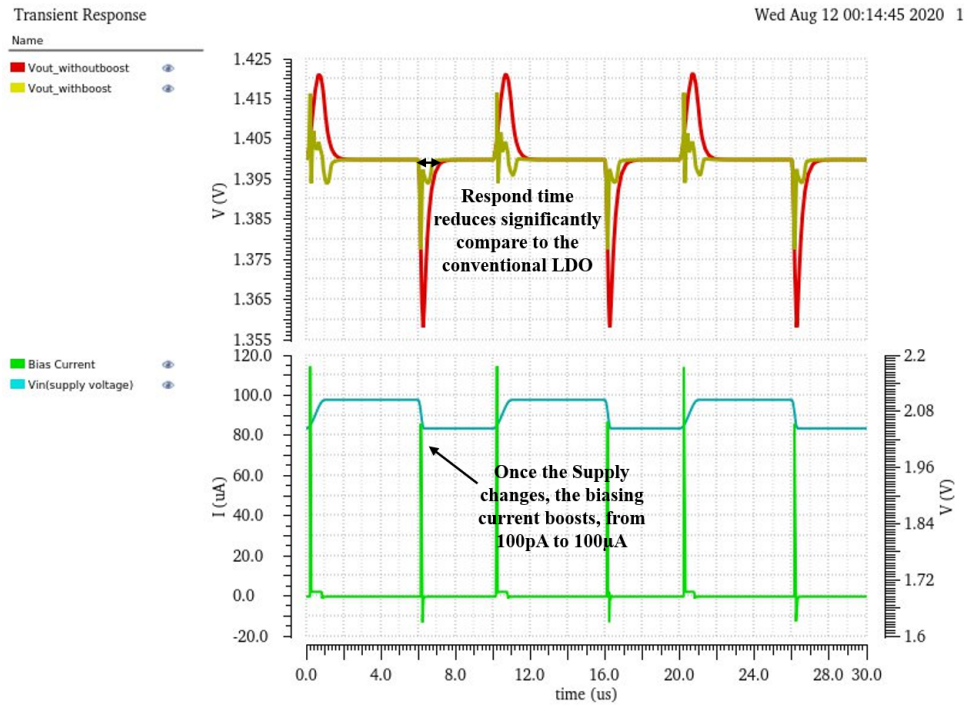



Figure 4.25: The comparison of LDO with and without proposed bias boost technique.

The Figure 4.25 shows the waveform of LDO with (yellow line) and without (red line) proposed bias boost technique. The low to high response time improves from $1.9\mu s$ to $1.1\mu s$ and the output high to low response time reduces from $1.8\mu s$ to $234ns$. The output fluctuation also decreases from $24mV$ to $5mV$. The bias current (green line) boosts from

$300pA$ to $100\mu A$ for $5ns$. This block consumes $23\mu W$ at steady state.

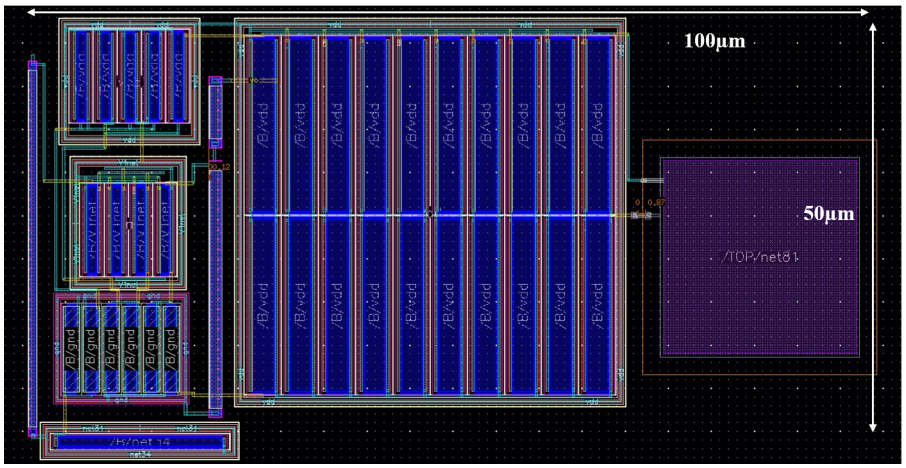



Figure 4.26: The layout diagram of self-tuned LDO.

Figure 4.26 shows the layout diagram of the self tuned LDO. The post layout co-simulation with BGR with respect to time is shown in the Figure 4.27. After considering the layout parameter, the LDO output increases to $1.42V$.

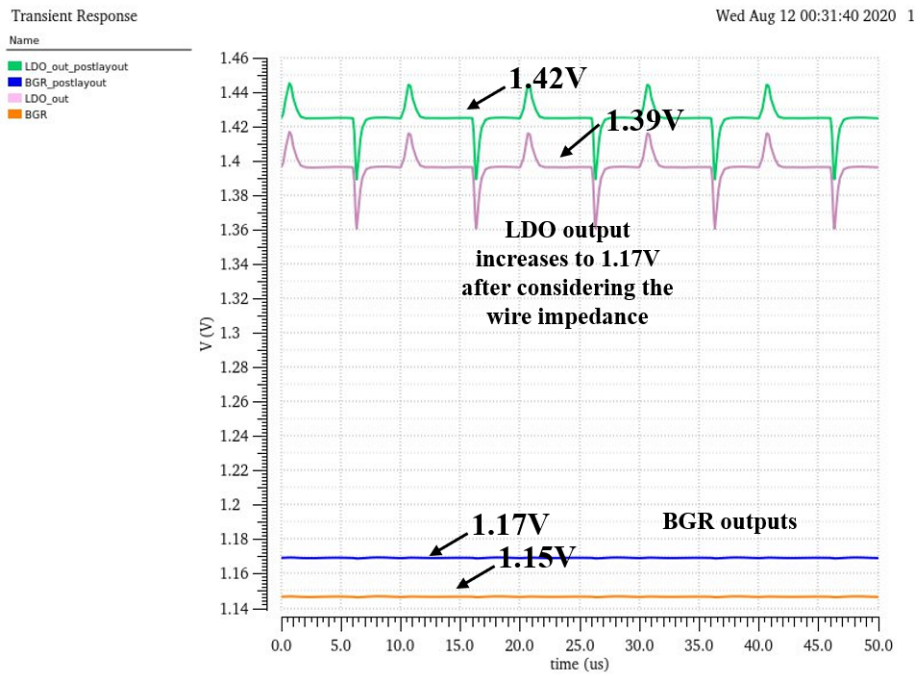



Figure 4.27: The post layout co-simulation of LDO with BGR with respect to time.

Figure 4.28 shows the AC response of the LDO and BGR before and after the post-layout simulation. There is no obvious deviation between them and the performance degrades above $100KHz$. But PSRR performance improves again at a higher frequency, above $500KHz$. The explanation is that the capacitors at high frequency are ignored and the miller compensation capacitor in the Opamp is shorted.

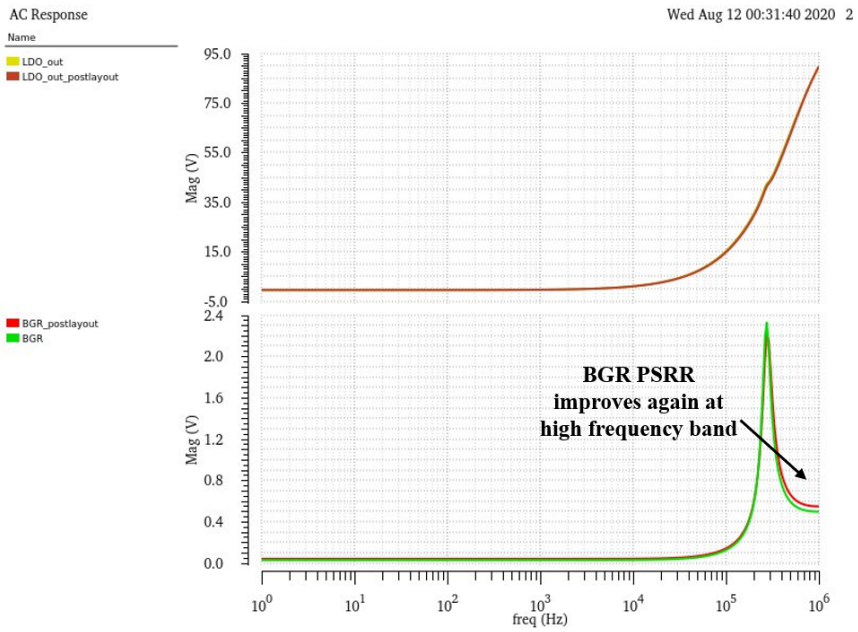



Figure 4.28: AC response of the LDO and BGR co-simulation before and after post-layout extraction.

## 4.5 Power On Reset

### 4.5.1 Theory

Power On Reset circuit plays a crucial role in WPDT system, ensuring the system work at a known state when it detects the power applied to the chip. When an IC system is power on, some of the internal nodes will settle to an unknown state and some capacitor may still store some residual charge. This uncertain possibility is not desirable for a WPDT system. Thus a POR circuit is introduced to produce a reset pulse signal in response to the initial power.

### 4.5.2 State of The Art

A Traditional POR is fundamentally a threshold level detection [42], shown in Figure 4.29.

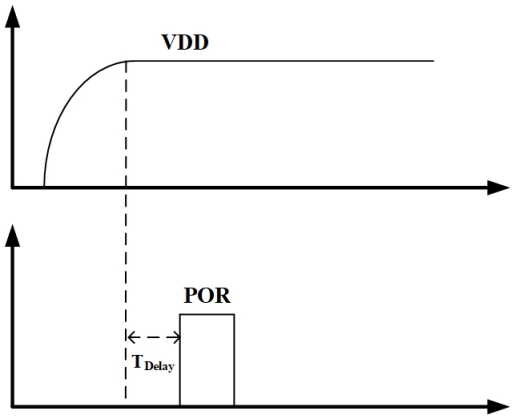



Figure 4.29: A POR pulse will trigger by a threshold level detection.

Huy-Binh Le proposed a long reset time POR based on threshold level detection which only consumes $1\mu A$ under $1.8V$ supply and occupies a $0.012mm^2$ area. However, this technique suffers from high design cost and area cost since it needs to redesign to adjust the threshold level. Another popular technique is applying a delay element in POR circuit to generate a delayed pulse [43]. But the conventional delay-element-based POR is not suitable in biomedical devices due to limited operation range, large quiescent current and limited supply voltage operation. Suat U. Ay [43] proposed an ultra-low power POR delay element only made up of two transistors and three capacitors.

### 4.5.3 Design Constraints

In this system, a POR reset is needed for the Dapper sensor, where the capacitors should be discharged once the circuit begins to work. But any interference between the POR circuit and the power management system is not allowed. A buffer or an automatic off block should be included in this POR circuit. The circuit should consume $\mu W$ level power and occupy a small area. It also needs to be able to detect false power on and power off signal.

### 4.5.4 Proposed POR Circuit

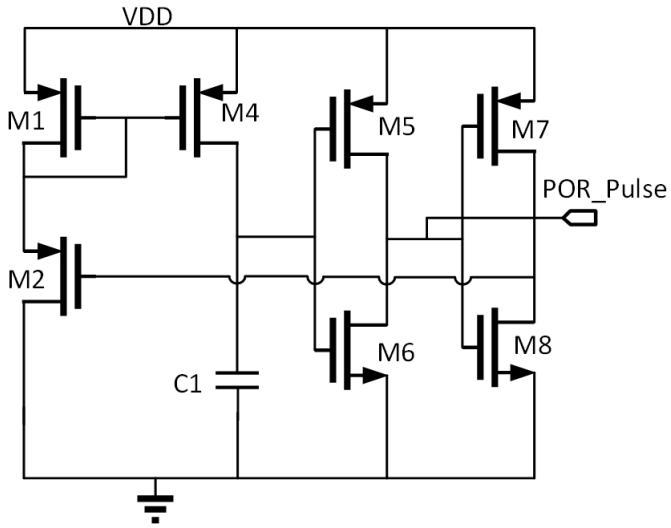



Figure 4.30: Schematic diagram of the proposed POR circuit

Figure 4.30 shows the schematic diagram of the proposed POR circuit. When the power is initially applied, there is no charge stored on the C1 and its potential level is low, which pushes the inverter M5-M6 to have a high level output at the beginning. Then $C1$ is charged via M4 once the power is on. When the potential level is charged higher than the switching point of the inverter, made up of M5 and M6, this inverter will output a low level potential. Meanwhile, a long delay inverter M7-M8 will shut the M2 off, thus there is no current flowing through M2 and M4, as M4 mirrors M1's current. Then this circuit is shut off and the capacitor holds the potential to ensure POR signal is low. The sizes of transistors are chosen such that they consume small power and small area. The capacitor is set to be $1pF$ so that the POR pulse can last around $1\mu s$.

### 4.5.5 Simulation and Layout

Figure 4.31 shows the waveform of the POR circuit. The green line is the power supply while the red line is the POR pulse signal. The POR circuit will generate a POR pulse once the supply initially is applied. The pulse will be high for $1\mu s$ and then become low. It can also be noticed that a supply fluctuation is ignored because the charged stored at the

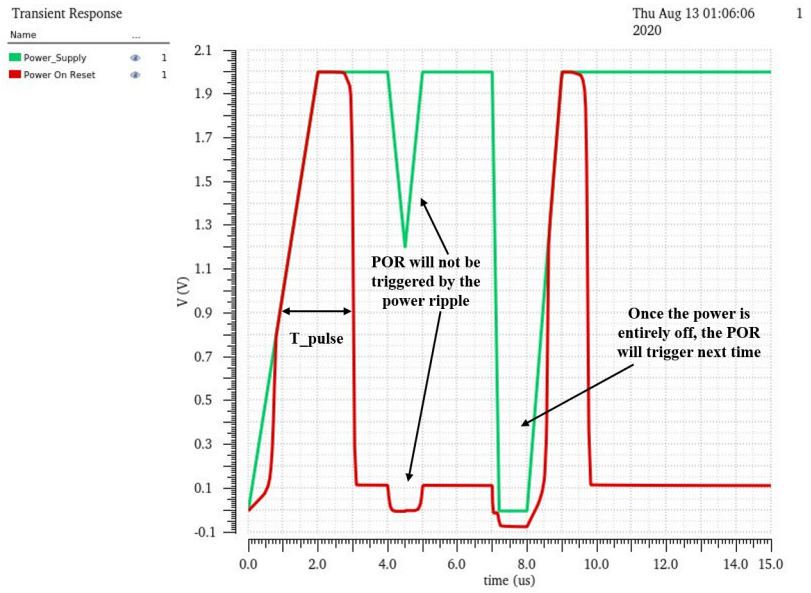



Figure 4.31: Waveform of the POR circuit. the red line shows the POR signal and green line show the power supply.

capacitor still holds. Only when the supply voltage decreases below the threshold voltage of the inverter, around $900mV$ in this design, the POR will restart.

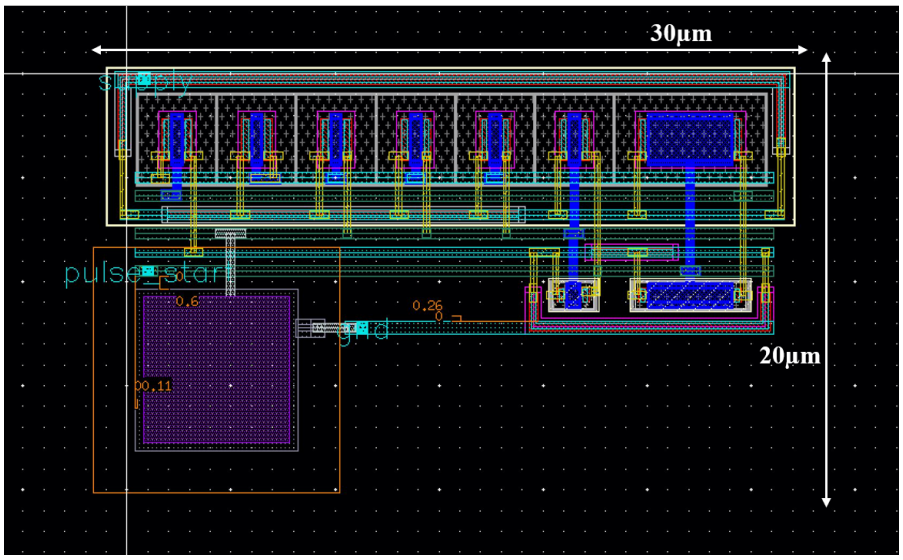



Figure 4.32: Layout diagram of the POR circuit.

Figure 4.32 shows the layout of the POR circuit. All the PMOS and NMOS are protected by the guard ring. The post-layout simulation is shown in the Figure 4.33. The

parasitic parameters did not affect the circuit too much.

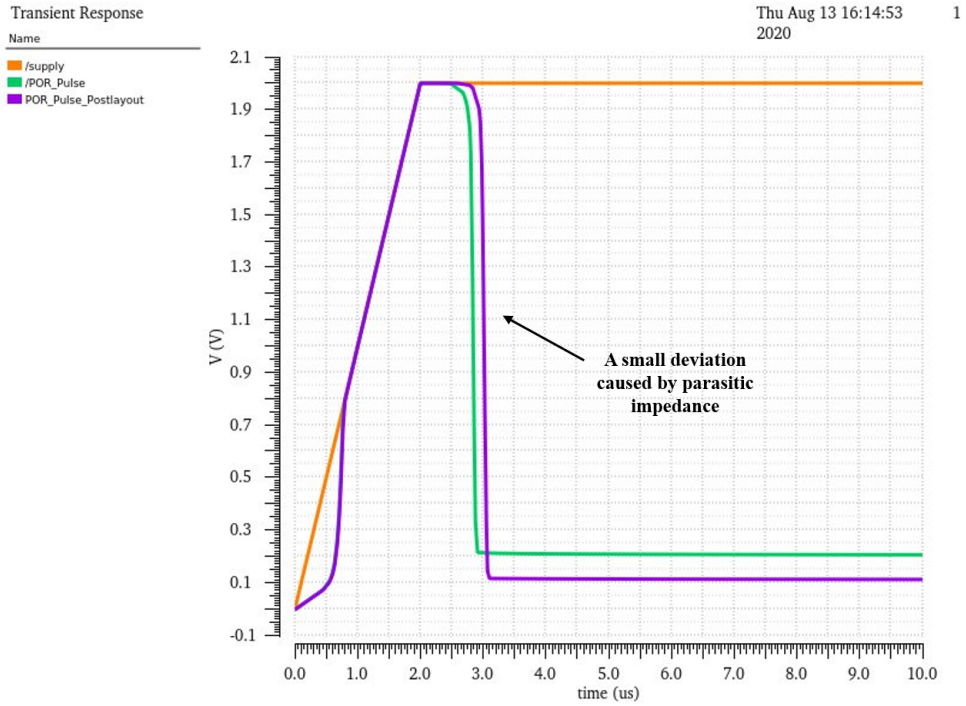



Figure 4.33: Post-Layout simulation of the POR circuit.

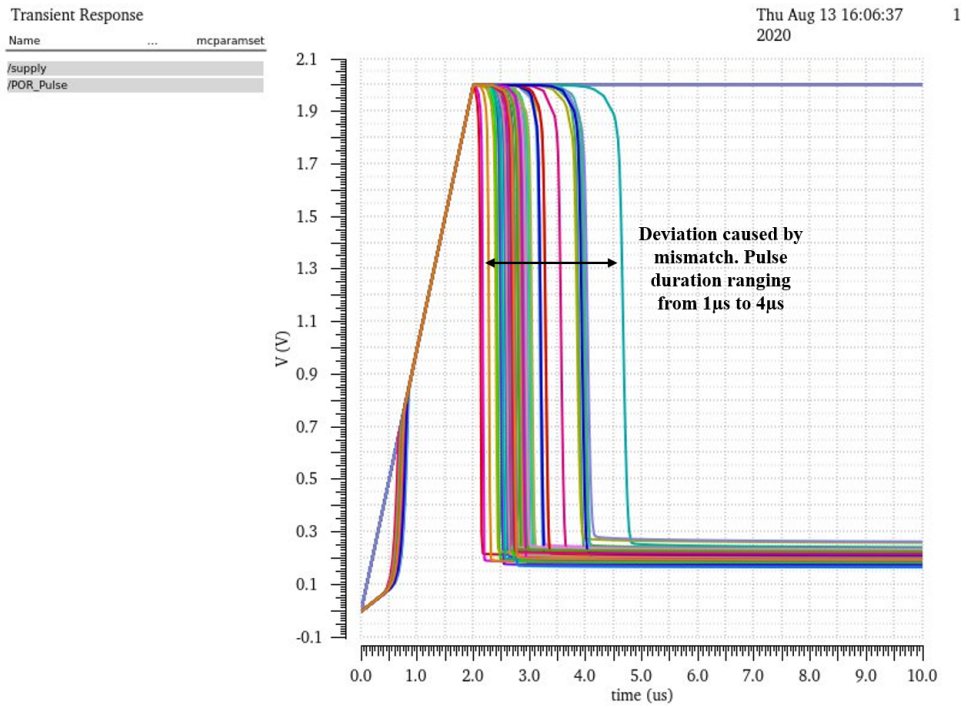



Figure 4.34: 50 runs of Monte Carlo simulation of POR.

The Monte Carlo simulation is shown in the Figure 4.34, There are 50 runs in total executed. All POR pulses can be generated while the pulse width differs from $600ns$ to $2.6\mu s$.

# Chapter 5

# Data Transmission System Implementation

## 5.1 Ion-Sensitive Field-Effect Transistor Sensor

### 5.1.1 Theory

ION-SENSITIVE field-effect transistor (ISFET) have played an important role in CMOS-based chemical sensing application since 1970s [5]. The implementation of large scale implementation has advantages of 1) robustness, 2) low cost and 3) scalability [44]. ISFET fundamentally is a MOSFET with the gate replaced by a reference electrode sensitive to ions in an aqueous solution [5].

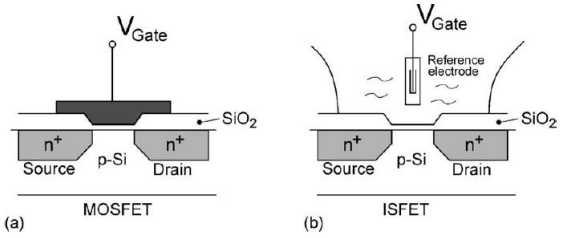



Figure 5.1: Schematic of MOSFET and ISFET [5].

To analyse ISFET, we have to understand the principle of MOSFET first. The

drain current of a standard MOSFET in linear region is expressed as

$$I_{\mathrm{d}} = C_{\mathrm{ox}}\mu\frac{W}{L}\left[\left(V_{\mathrm{gs}} - V_{\mathrm{t}}\right)V_{\mathrm{ds}} - \frac{1}{2}V_{\mathrm{ds}}^2\right] \tag{5.1}$$

where $C_{ox}$ is the oxide capacitance per unit, W and L are the width and the length of the transistor and $\mu$ is the carrier's mobility. $V_t$ is the threshold voltage, which can be expressed as

$$V_{\mathrm{t}} = \frac{\Phi_{\mathrm{M}} - \Phi_{\mathrm{Si}}}{q} - \frac{Q_{\mathrm{ox}} + Q_{\mathrm{ss}} + Q_{\mathrm{B}}}{C_{\mathrm{ox}}} + 2\phi_{\mathrm{f}} \tag{5.2}$$

where $\Phi_M$ and $\Phi_{Si}$ are the work function of gate metal and silicon respectively, $q$ is the charge, $Q_{ox}$, $Q_{ss}$ and $Q_B$ are the charge in the oxide, charge in the oxide-silicon interface and depletion charge, and $\phi_f$ is the surface potential. While in the ISFET, part of the threshold voltage remains the same while two more parameters are brought in: the potential of reference electrode $E_{ref}$ and interface potential between under-test-solution and oxide $\Psi + \chi^{sol}$, which are determined by the pH solution. Then $V_t$ can be expressed as:

$$V_{\mathrm{t}} = E_{\mathrm{ref}} - \Psi + \chi^{\mathrm{sol}} - \frac{\Phi_{\mathrm{Si}}}{q} - \frac{Q_{\mathrm{ox}} + Q_{\mathrm{ss}} + Q_{\mathrm{B}}}{C_{\mathrm{ox}}} + 2\phi_{\mathrm{f}} = f(pH) \tag{5.3}$$

As a result, drain current $I_d$ can be expressed as a function of pH.

### 5.1.2 Amperometric Implementation

There are many ISFET readout circuits based on standard CMOS technology have been published over the decades [44]. Most of them use Opamps to fix ISFET's terminals potential to read the data. B. Premanode proposed a current feedback readout [45] and Pookaiyaudom proposed an adapted current conveyor for ISFET readout [46]. In this system, a capacitor integrator amperometric is applied to convert the ISFET current to a digitised square wave, which can be mixed with another Potentiometric signal. The schematic in the Figure 5.2 shows the structure of the amperometric circuit, which will generate a square wave corresponding to the input current magnitude. It consists of a capacitor integrator, comparator and an OR gate. The capacitor will be discharged at the reset state, and then the current will charge the capacitor, raising up the $INT\_OUT$. Once

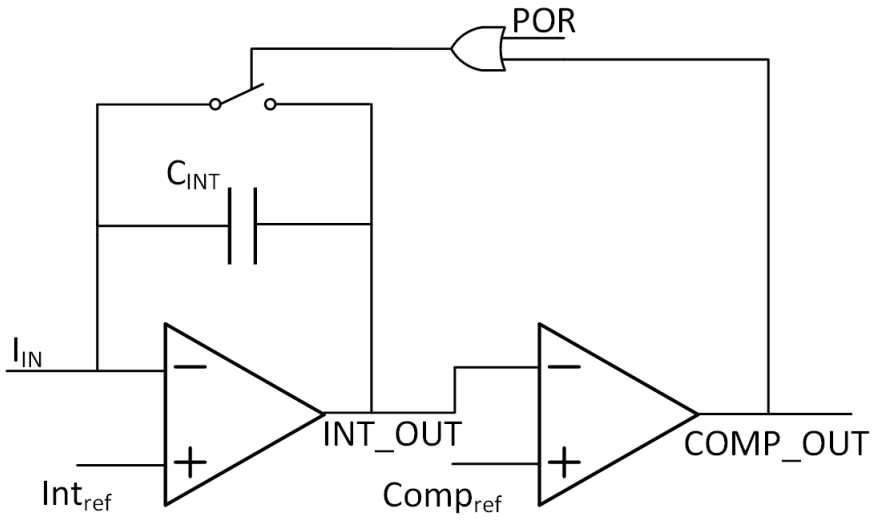



Figure 5.2: Schematic of amperometric readout circuit.

the $INT\_OUT$ is higher than another input terminal of the comparator, the $COMP\_OUT$ will be high, and the switch S1 will close and discharge the capacitor. After a short period of propagation delay, the $INT\_OUT$ will reset to be same as $INT\_ref$. The simulation is shown in the Figure 5.3.

The frequency of the square wave is given by [2]:

$$F_{DFF} = \frac{1}{T_{DFF}} = \frac{1}{2(t_{pd} + t_{int})} \tag{5.4}$$

where $t_{pd}$ is the propagation delay, $t_{int}$ is the integrating time, which can be express as:

$$t_{int} = \frac{C_{INT}\Delta V}{I_{in}} \tag{5.5}$$

Thus the frequency can be expressed as:

$$F_{DFF} = \frac{I_{in}}{2(t_{pd}I_{in} + C_{INT}\Delta V)} \tag{5.6}$$

The capacitor is chosen as $0.5pF$ such that the area occupancy is small and the output frequency ranges from $0 - 300KHz$ at an input current range of $80pA - 1\mu A$ .

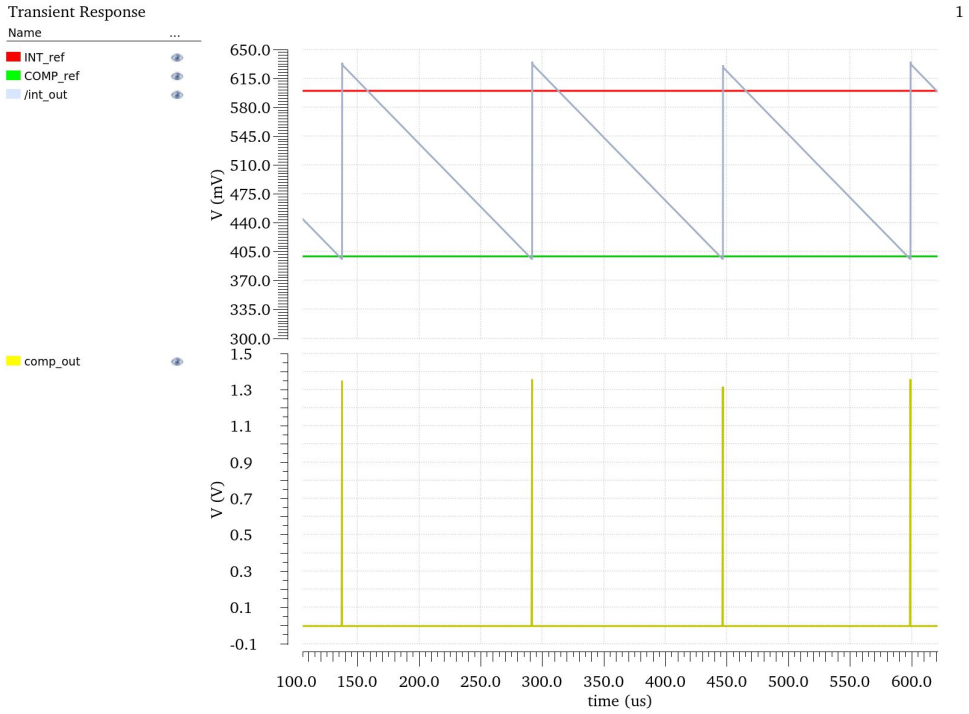



Figure 5.3: Waveform of the amperometric circuit. The comparator output triggers once the integrator output reduces below $COMP\_ref$.

## 5.2 Potentiometric circuit

This potentiometric circuit is fundamentally an ion-selective electrode and a voltage controlled oscillator, responsible for converting the voltage to a square wave.

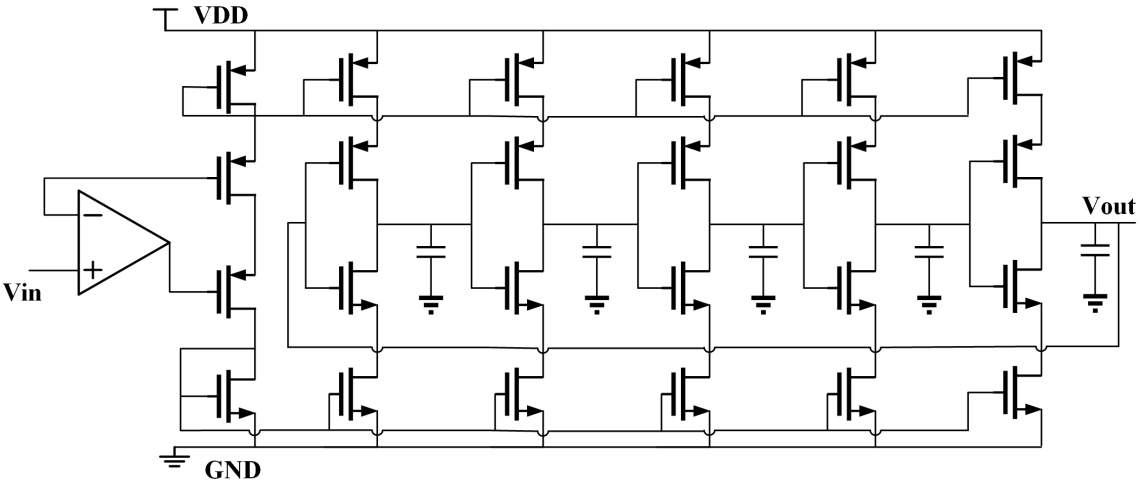



Figure 5.4: Schematic diagram of the voltage controlled oscillator.

Figure 5.4 shows the schematic of the voltage controlled oscillator (VCO) where $Vin$ connects to the Ion-selective electrode. The frequency of the square wave is determined by the ring oscillator equation:

$$f = \frac{1}{T} = \frac{1}{2Nt_d} \tag{5.7}$$

where $N$ is the stage number of the oscillator, $t_d$ is the delay time of each stage, which can be expressed as

$$t_d = \frac{CV_{cap}}{I_d} \tag{5.8}$$

The magnitude of $Vin$ will decide how much current $I_d$ will flow through the ring oscillator via the current mirror, and decide the square wave frequency. There is an addition capacitor added after each stage of oscillator, further reducing the $t_d$ of each stage, and reduce the power consumption as well. The size of all the PMOS and NMOS are set such the length is big and width is small to decrease drain current as well as power consumption. The simulation waveform is shown in the Figure 5.5. A square wave is generated at a frequency of $5Hz$ as the input is $700mV$.

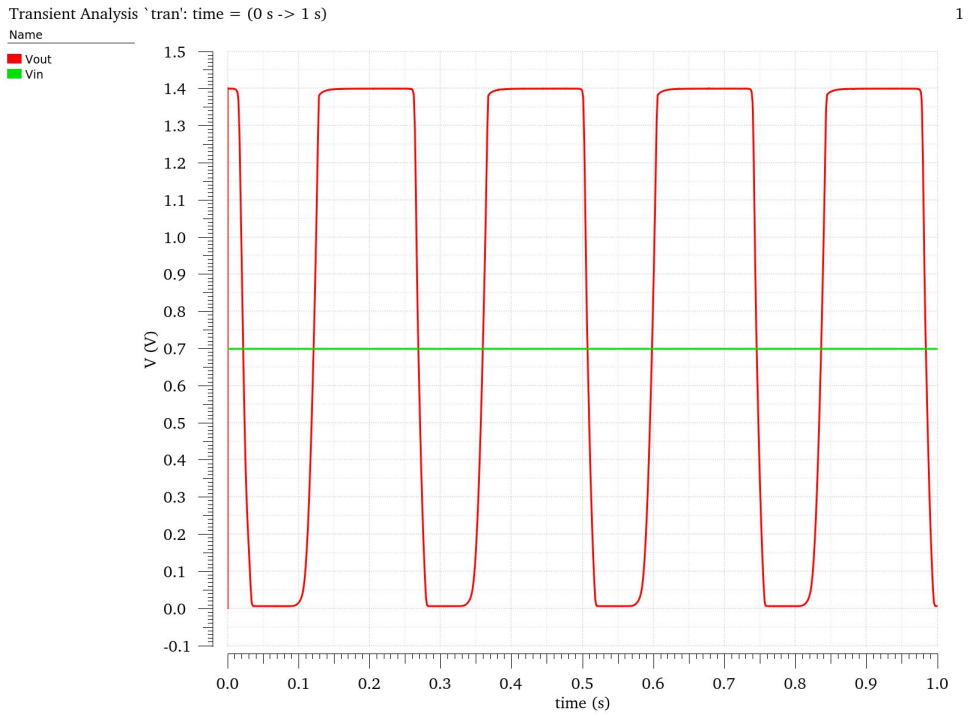



Figure 5.5: Simulation waveform of the voltage controlled oscillator. Voltage input is converted to a square wave with a certain frequency.

## 5.3 Data Mixing Modulator

A simple and low-power D flip flop is used to mix the high frequency amperometric signal and the low frequency potentiometric signal, shown in the Figure 5.6:

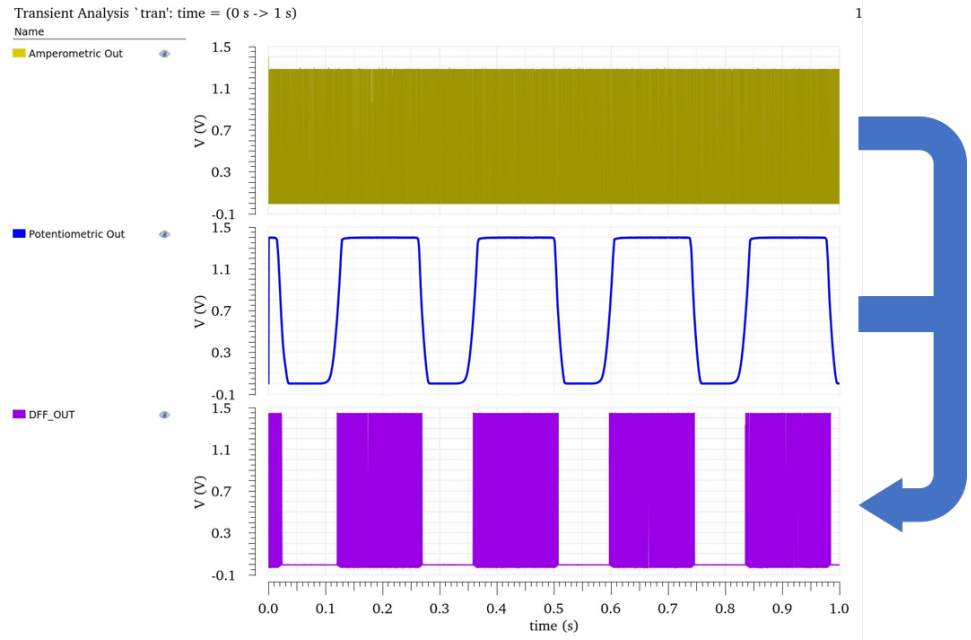



Figure 5.6: Simulation waveform of the Dapper Sensor. The output signal mixes the amperometric signal and the potentiometric signal

After obtaining the digitised data, the next step is to transmit the information to the external circuit.

## 5.4 Data transmission technique

### 5.4.1 Theory and state of the art

Wireless data transmission techniques are essential in biomedical implanted systems. The most commonly used techniques are Amplitude shift keying (ASK), Phase shift keying (PSK) and Frequency shift keying (FSK). The system approach selection depends on several parameters: bandwidth efficiency, power efficiency and bit error rates [47]. Bandwidth efficiency stands for the technique's ability to wisely use the limited frequency bandwidth. Power efficiency represents the technique's ability to transmit the data to the external

circuit without interfering the wireless received power. The bit error rate measures the systems' transmission error due to the noise and interference.

### Amplitude Shift Keying

Amplitude Shift Keying is widely used in radiotelegraphy, industrial networks devices and wireless base stations, where the carrier amplitude changes according to a digital input signal. An example of an input and the modulated signal is shown in the Figure 5.7.

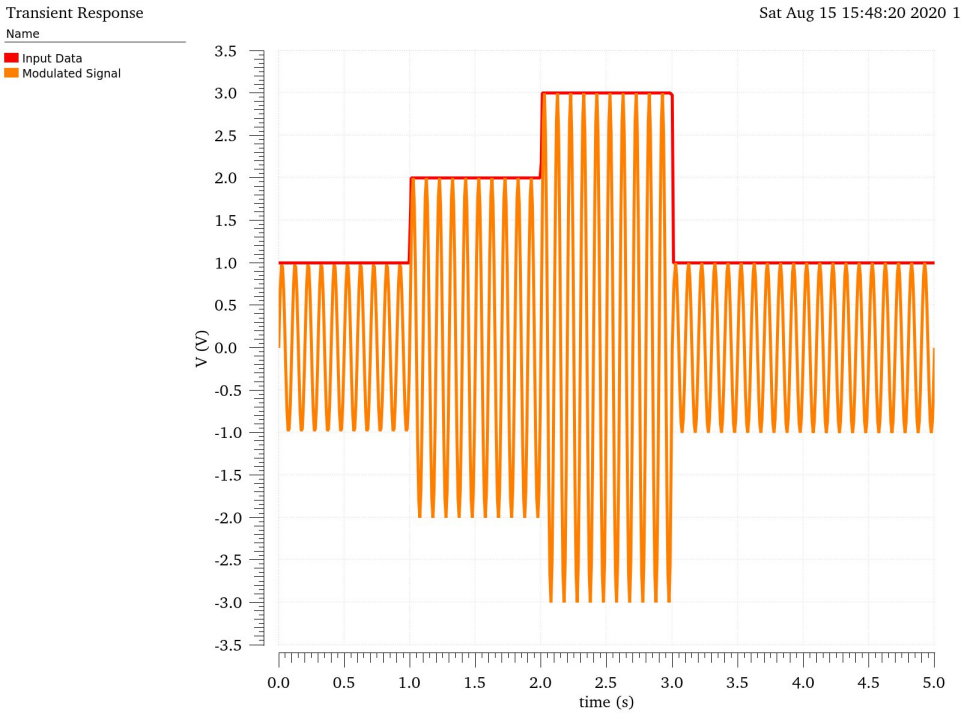



Figure 5.7: An example of ASK modulation. The carrier amplitude changes according to a digital input signal. The modulation technique buries the digitised data in the envelop of the carrier signal.

The modulation technique buries the digitised data in the envelop of the carrier signal, which is more sensitive to noise and requires linear amplifier. The mathematical equation of M-bit ASK can be expressed as:

$$V_{ASK}(t) = A_m \cos(2\pi f_c t) \quad A_m \in (2m - 1 - M)\Delta \tag{5.9}$$

where $m = 1, 2, ...M$. A special form of ASK is on-off keying (OOK), which can be

expressed as:

$$V_{ASK}(t) = \begin{cases} 0, & \text{Vin} = 0 \\ A * \cos(2\pi f t), & \text{Vin} = 1 \end{cases} \tag{5.10}$$

This special OOK can be easily implemented using an on-off switch. ASK has advantages over other wireless techniques that it allows to demodulate the envelope of the carrier signal in low power applications, since envelope detection is easy to implement and low power. Besides, it does not require frequency conversion blocks such as phase-locked-loop, which is complex and area-consuming and not desirable in WPDT system.

### Frequency Shift Keying

Frequency Shift Keying is a wireless modulation scheme where digital information is transmitted via frequency change. This scheme is commonly used in telemetry and low frequency radio systems. Even now FSK is also the main scheme of radio broadcasting. Frequency modulation encodes the digitised data in a changed frequency signal with a constant amplitude. An example of an FSK is shown in the Figure 5.8:

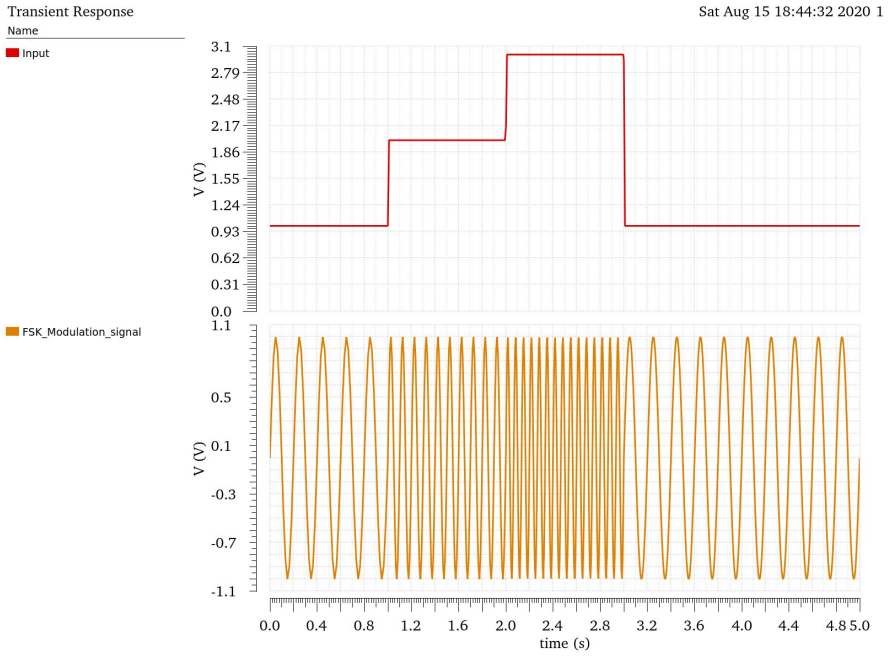



Figure 5.8: An example of FSK modulation. The carrier frequency changes according to a digital input signal.

The M-bit FSK can be expressed as:

$$V_{FSK}(t) = A * cos(2\pi(f_c + m\Delta f)t) \tag{5.11}$$

where $m = 1, 2, ...M$. The FSK benefits from less distortion from amplitude and non-linear amplifier can be used with less power consumption. However, in our body dust system, the power and data are transmitted through a singer inductive coil and the RF frequency is set to be resonant frequency where the power transmission efficiency is maximum. The frequency modulation will degrade the PCE, thus FSK is not suitable in this WPDT system.

### Phase Shift Keying

Phase shift keying is another popular wireless data transmission technique where the carrier signal phase is varied with respect to the digitised data.

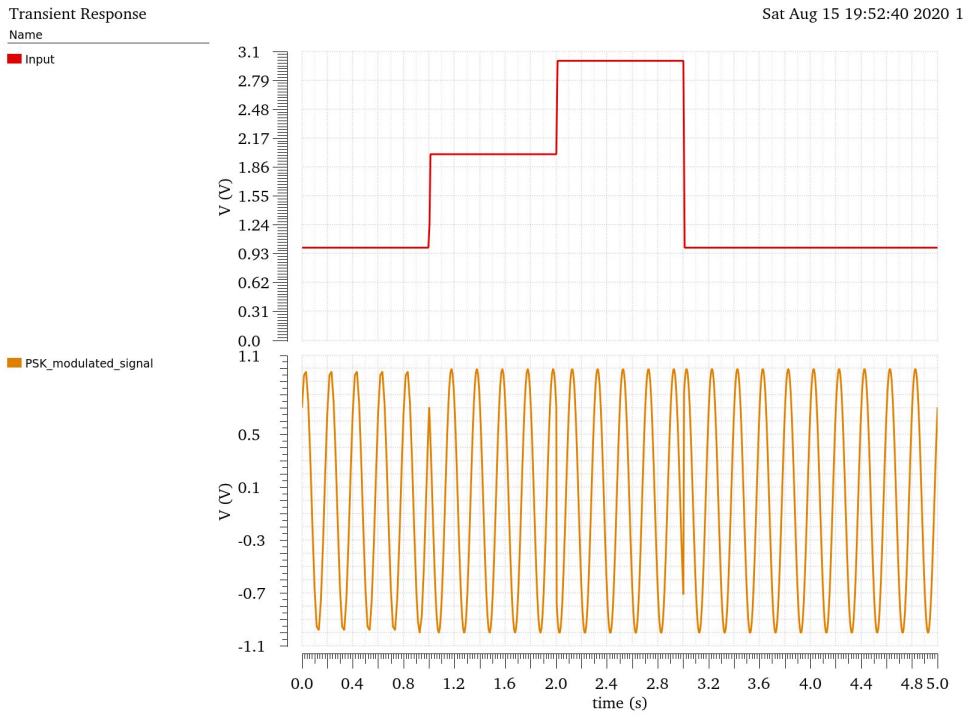



Figure 5.9: An example of PSK modulation. The carrier signal phase is varied with a digital input signal.

M-bit PSK can be mathematically expressed as:

$$V_{PSK}(t) = Acos(wt - \Phi_m(t)) \tag{5.12}$$

where $\Phi_m(t) = \frac{2\pi m}{M}$, $m = 1, 2, ...M$. PSK has a better performance than ASK and FSK but requires complex phase detection blocks. In the case the input data is only 2-bit and the phase of the carrier signal separates by 180°, the scheme is called as Binary Phase Shift Keying (BPSK).

### 5.4.2 Load Shift Keying

However, all three schemes stated above suffer from complexity, big area occupancy and low power efficiency in WPDT system. A new data transmission scheme, load shift keying, is introduced recently to tackle these issues. LSK is a special form of ASK, also referred as reflected modulation or back-scattering [48], to modulate resonant capacitance or resistance of the secondary side circuit. The principle is that a resonant frequency shift, caused by the load impedance change at the secondary side circuit, can be reflected back at the primary side and be observed as a voltage change across the coil [49]. The easiest way to perform LSK is to use a switch to short a series resistor or a parallel capacitor.

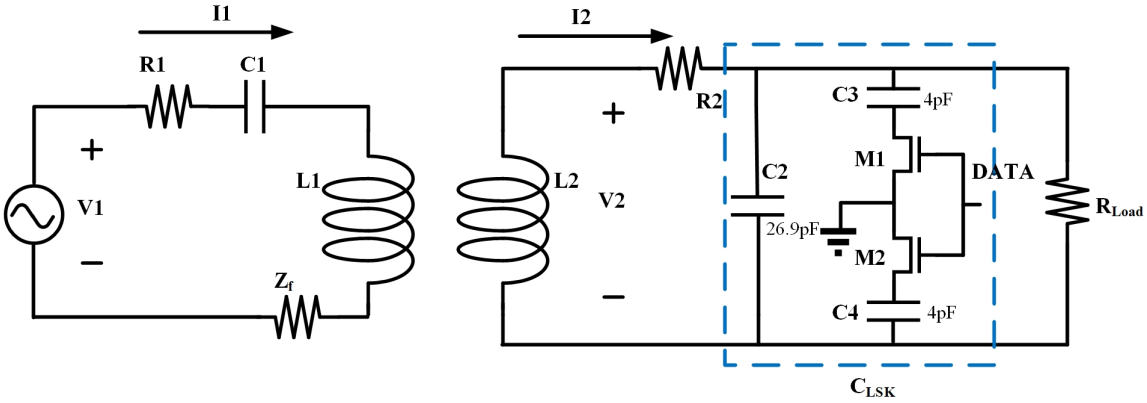



Figure 5.10: The Schematic diagram of LSK circuit.

The Schematic diagram of LSK circuit is shown in the Figure 5.10. $Z_f$ is the equivalent impedance of the second side coil seen at the primary side, which can be expressed

as:

$$Z_f = \frac{(\omega M)^2}{Z_2} \tag{5.13}$$

where $Z_2$ is the equivalent impedance of the second side circuit, $M$ is the mutual impedance which equals $k(L_1L_2)^{\frac{1}{2}}$ and $\omega$ is the angular frequency of the RF signal. The load impedance at the second side can be expressed as :

$$\begin{aligned} Z_2 = \frac{V_2}{I_2} &= j\omega L_2 + R_2 + (\frac{1}{R_{Load}} + j\omega C_{LSK})^{-1} \\ &= j\omega L_2 + R_2 + \frac{R_{Load}(1 - j\omega C_{LSK} R_{Load})}{1 + \omega^2 C_{LSK}^2 R_{Load}^2} \\ &= R_2 + \frac{R_{Load}}{1 + \omega^2 C_{LSK}^2 R_{Load}^2} + j(\omega L_2 - \frac{\omega C_{LSK} R_{Load}^2}{1 + \omega^2 C_{LSK}^2 R_{Load}^2}) \end{aligned} \tag{5.14}$$

Similarly, the impedance at the first side is given by:

$$Z_1 = \frac{V_1}{I_1} = R_1 + Z_f + j(\omega L_1 - \frac{1}{\omega C_1}) \tag{5.15}$$

To increase the PTE of the coil, both sides circuits are operating at the resonant frequency, which means the imaginary part is zero:

$$j(\omega L_2 - \frac{\omega C_{LSK} R_{Load}^2}{1 + \omega^2 C_{LSK}^2 R_{Load}^2}) = 0 \tag{5.16}$$

$$j(\omega L_1 - \frac{1}{\omega C_1}) = 0 \tag{5.17}$$

Equation 5.16 can be expressed as :

$$\frac{1}{1 + \omega^2 C_{LSK}^2 R_{Load}^2} = \frac{L_2}{C_{LSK} R_{Load}^2} \tag{5.18}$$

And then Equation 5.14 can be simplified as :

$$Z_2 = R_2 + \frac{L_2}{C_{LSK} R_{Load}} \tag{5.19}$$

By combining all the equations, we obtain:

$$\begin{aligned} Z_1 = R_1 + Z_f &= R_1 + \frac{(\omega M)^2}{Z_2} \\ &= R_1 + \frac{\omega^2 k^2 L_1 L_2}{R_2 + \frac{L_2}{C_{LSK} R_{Load}}} \\ &= R_1 + \frac{\omega^2 k^2 L_1 L_2 C_{LSK} R_{Load}}{R_2 R_{Load} C_{LSK} + L_2} \end{aligned} \tag{5.20}$$

Define $V_{L1}$ as the absolute voltage across the first side coil, we obtain :

$$\begin{aligned} V_{L1} &= \frac{\omega L_1}{Z_1} V_1 \\ &= \frac{\omega L_1 V_1}{R_1 + \frac{\omega^2 k^2 L_1 L_2 C_{LSK} R_{Load}}{R_2 R_{Load} C_{LSK} + L_2}} \end{aligned} \tag{5.21}$$

If a digitised data from Dapper sensor controls the NMOS switch of the LSK, then the $C_{LSK}$ will change to $C'_{LSK}$. Then:

$$V'_{L1} = \frac{\omega L_1 V_1}{R_1 + \frac{\omega^2 k^2 L_1 L_2 C'_{LSK} R_{Load}}{R_2 R_{Load} C'_{LSK} + L_2}} \tag{5.22}$$

Thus the voltage change across the primary coil can be observed and data can be recovered.

However, In this Body Dust system, the data transmission link shares the same coil with the powering link. When the load capacitance changes, the power transmission efficiency might decrease. An appropriate LSK capacitance value should achieve in order to have enough voltage shift at the primary side for being observed and recovered, and also maintain the high PTE. In order to find the best balance, the voltage shift across the primary coil (dashed line) and power efficiency degradation are plotted as a function of LSK capacitance, shown in Figure 5.11. $C_3$ and $C_4$ are chosen to be $3pF$, and voltage will shift $1.1V$ and PTE will have 70% maximum performance.

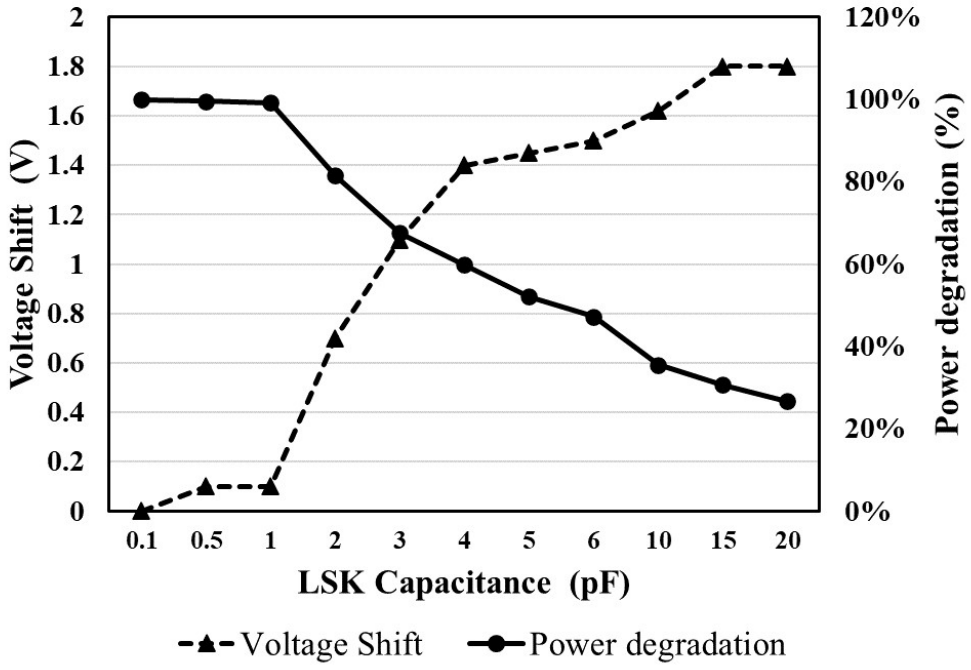



Figure 5.11: The line diagram of Voltage shift and PTE degradation with respect to different LSK Capacitance. When $C_3$ and $C_4$ in Figure 5.10 equal to $3pF$, they achieve the best balance between voltage shift and PTE

### 5.4.3 Simulation and Layout

Figure 5.12 shows the simulation transient waveform of the applied LSK circuit. Once an LSK data triggers the LSK switch, a voltage shift across the primary side can be observed.

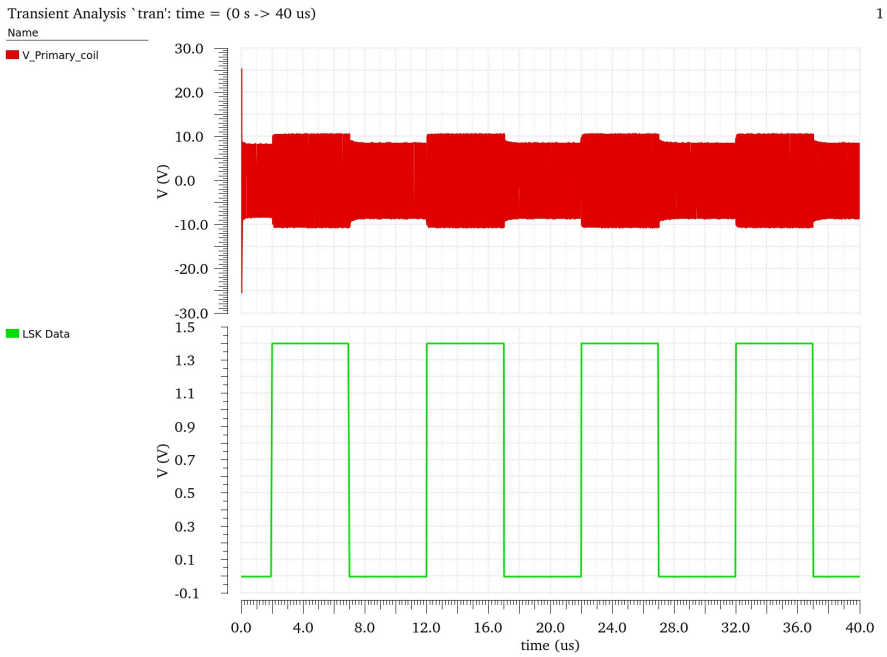



Figure 5.12: The simulation waveform of LSK circuit. Once an LSK data triggers the LSK switch, a voltage shift across the primary side can be observed.

The layout diagram of the LSK circuit is shown in the Figure 5.13. A large size NMOS switch is chosen to have a large parasitic capacitance in series with $C_3$ and $C_4$.

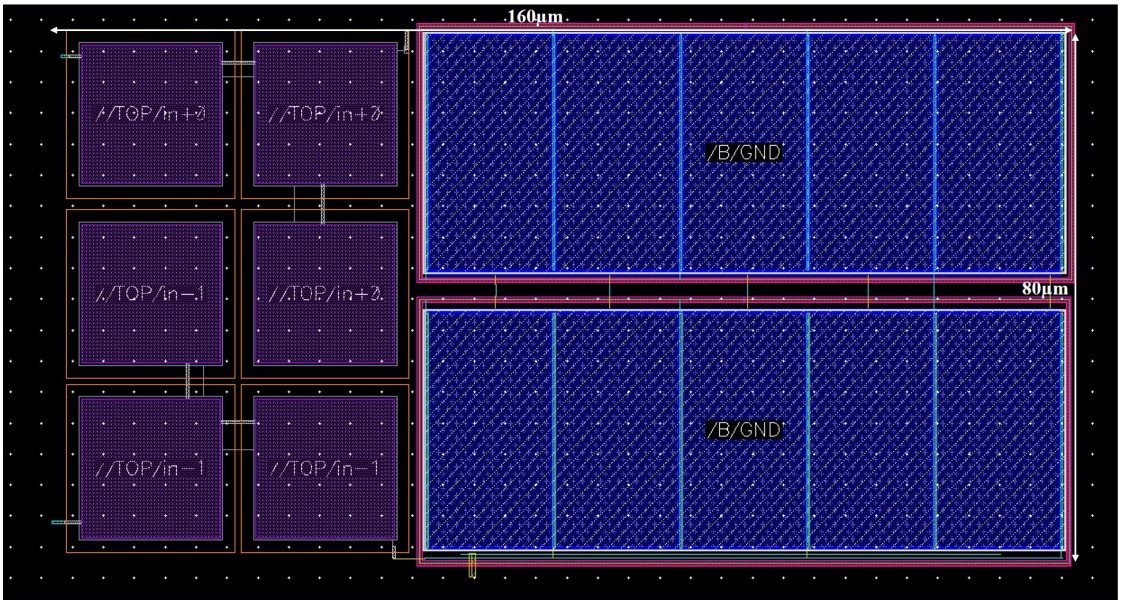



Figure 5.13: The layout diagram of the LSK circuit.

The post-layout simulation and the original simulation are compared. The voltage shift happens in $10ns$ after the LSK triggers.

# Chapter 6

# Overall System Results and Test Consideration

## 6.1 System Simulation

THE body dust system level simulation is shown in the Figure 6.1. Firstly the power is transmitted from the first side coil to the rectifier at the second side coil, and it takes BGR and LDO $8\mu s$ and $4\mu s$ to settle respectively. POR pulse is generated only at the first $5\mu s$ to reset the Dapper sensor. When the $V_{in}$ is set to be $700mV$ and $I_{in}$ is $50nA$, the $LSK\_Data$ signal triggers at $10\mu s$ after a $5\mu s$ POR signal. The voltage generated by rectifier $V\_Rectifier$ fluctuates between $2.044V$ and $2.15V$ and the voltage provided by LDO $V\_supply\_1.4V$ decreases and recovered in $1\mu s$ at the time the $LSK\_Data$ flips. The bandgap voltage output $BGR$ remains constant with less than $1mV$ fluctuation all the time. Meanwhile, the load shift caused by $LSK\_Data$ at the secondary side circuit also reflects back at the primary side across the coil inductor, shown as $V\_first\_side$ in orange line. The voltage across the primary coil changes from $7V$ to $8.2V$ when $LSK\_Data$ goes from low to high and decreases back to $7V$ when $LSK\_Data$ goes down. Thus the data is successfully transmitted to the external circuit.

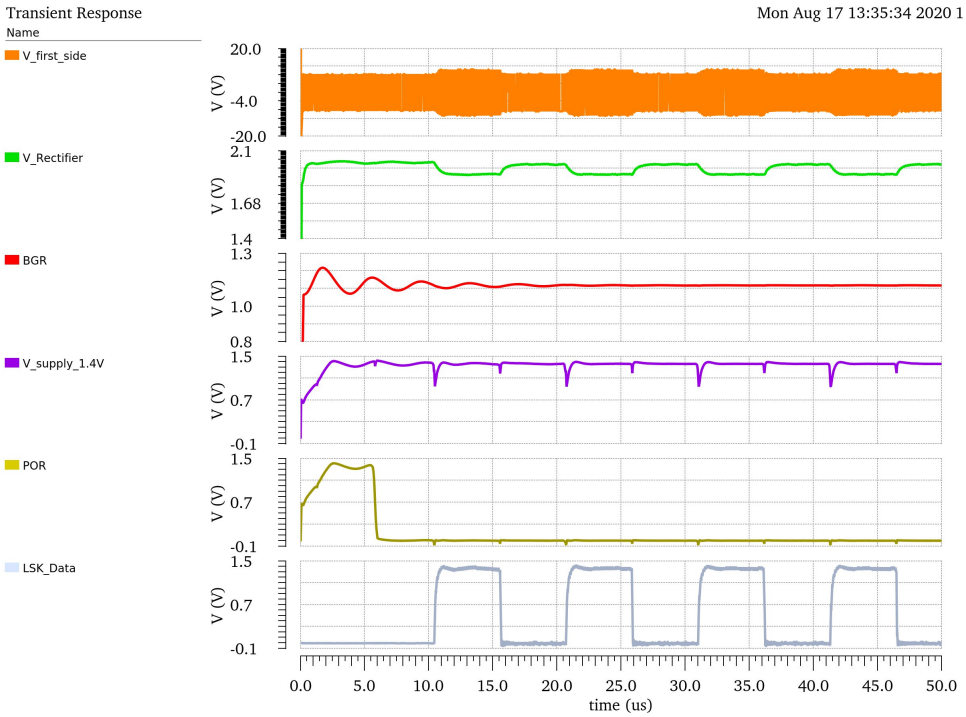



Figure 6.1: The Body Dust system level simulation diagram.

## 6.2 System layout and test point consideration

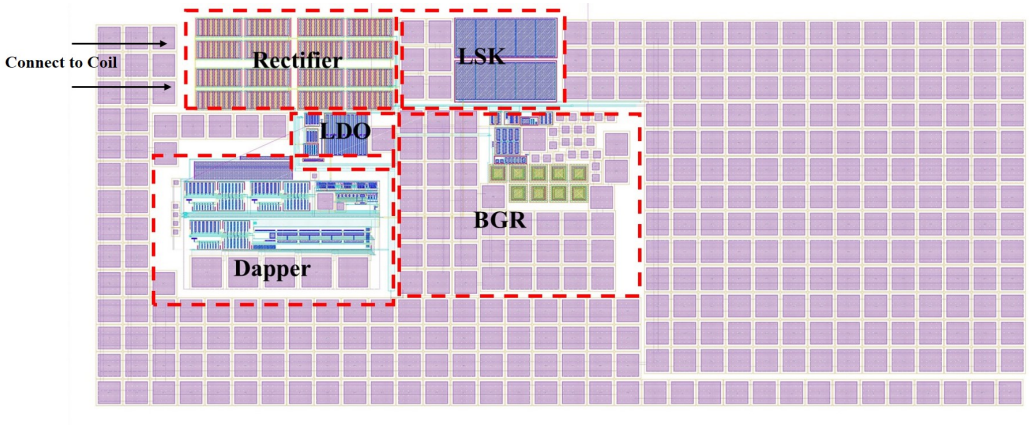



Figure 6.2: The Body Dust system layout. A large area smoothing capacitor is surrounding around the circuit.

Figure 6.2 shows the system layout diagram. All the blocks are placed in the position shown in the figure. The coil will connect to the rectifier, which is placed at the left

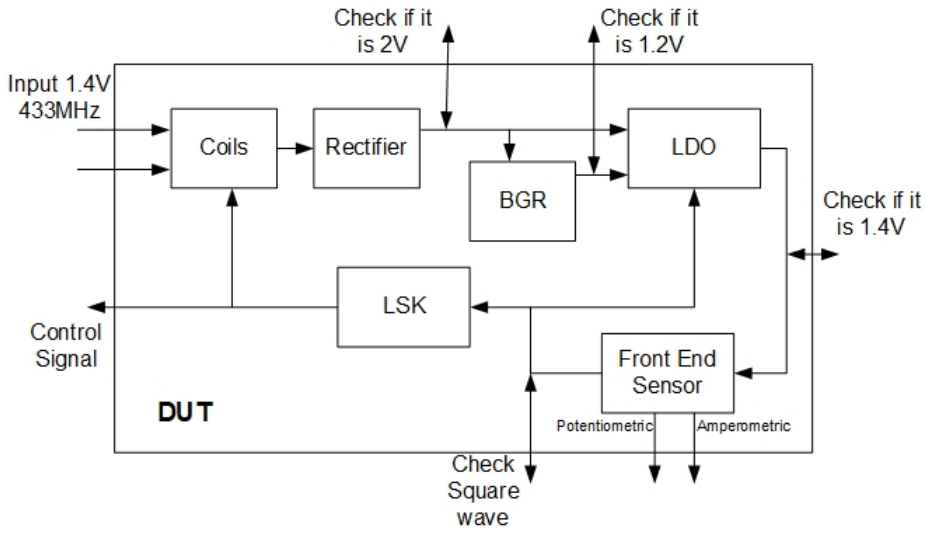



Figure 6.3: The Body Dust system test plan diagram.

top side of the system. The front end Dapper is placed using the shortest connected track metal, so that the internal track resistance is minimum. The rest of the circuit is the smoothing capacitor connected to the rectifier. There are additional test point pins placed in each block to be able to operate measurement test after fabrication, shown in the Figure 6.3. If some circuit blocks are failed, these test points allow detailed check and the failed blocks can be replaced by the additional commercial IC chip or independent voltage supply. However, these may require extra bond pads.

Figure 6.4 shows the flow chart of the system level test. The front end sensor and the power data management block will be tested independently firstly. An independent voltage source will supply the front end sensor via the test bond pad to check whether the front end sensor is able to generate a correct square wave signal. Meantime, each block will be tested sequentially to meet all the specification. If one block fails, an independent and commercial IC chip is utilised. Once circuits in both branches work, they will be combined together to validate the entire system's function. If a voltage shift, varied with the data, can be observed at the primary coil, the system proves to be work. Otherwise, the unsuccessful block should be redesigned and tested again.

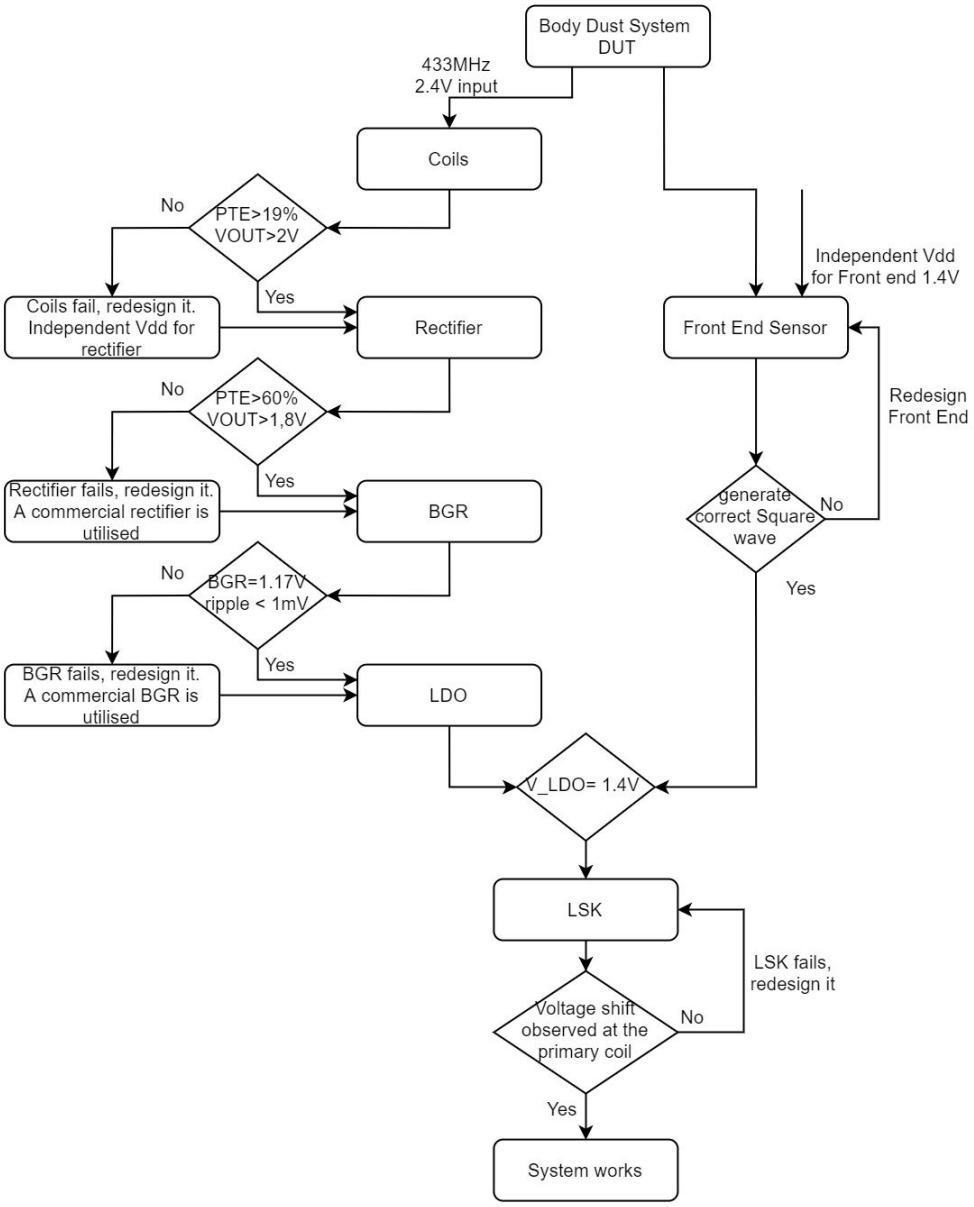



Figure 6.4: The Body Dust system test plan flow chart.

# Chapter 7

# Conclusion and Future work

## 7.1 Conclusion

THIS thesis has designed and implemented an electrochemical sensing system based on wireless data and power transmission technique using TSMC $0.18\mu m$ technique. This work will be fabricated and tested in the incoming September. Chapter One introduces the motivation of this work and the importance of WPDT system to Biomedical applications. Chapter two gives the background information of WPDT system for the past few decades and summarises the latest state-of-the-art technique. Then the general principle of power transmission and data transmission are discussed as well as the front end sensing approach. The system architecture overview is given in Chapter three, including the system's specification and objectives. Chapter four and five describe power and data transmission circuit block in detail respectively, including theory, state-of-the-art, design, simulation and layout. Chapter six gives the system level simulation and layout, and discusses the test point consideration.

In conclusion, this WPDT system successfully converts and transmits RF power to the internal circuit, and provides a $1.4V$ stable output voltage to the front end Dapper sensor, which is optimised to be low power and only consumes $11\mu W$.

The Dapper sensor is able to measure amperometric and potentiometric signal concurrently and mix them into a square wave signal with a frequency depending on the

voltage input and current input. Inside the WPDT system, the coil is designed to have a 19.2% PTE and rectifier has 62.1% of PTE at RF frequency $433MHz$. Due to the effect of LSK, a high PSRR BGR is required and the proposed BGR achieves a PSRR of $-60dB$ at $100KHz$ and provides a stable $1.14V$ supply. A novel bias boost LDO circuit is designed to only consume $23\mu W$ at steady state but have fast response time once the input changes. Different techniques are applied to the Dapper sensor to reduce the power consumption, such as fewer components, smaller bias current and less reference signal. The system successfully passed the post layout simulation and extra test point bond pads are placed. This body dust system is going to fabricate in the incoming September. The system characteristics is summarized in the Table 7.1.

A publication work is extracted from this work and attached in the Appendix B, and will be submitted to the IEEE conference ISCAS 2021.

Table 7.1: SYSTEM CHARACTERISTICS SUMMARY

| Parameter | Performance |
|---|---|
| System: | |
| Technology | TSMC 0.18$\mu m$ |
| Supply voltage(external circuit) | 2.4V |
| Data transmission technique | LSK |
| Coil dimension | $3mm * 3mm$ |
| WPDT system dimension | $936\mu m * 426\mu m$ |
| Power dissipation (WPDT) | $87\mu W$ |
| Power dissipation (Front end) | $11\mu W$ |
| Rectifier: | |
| Area | $200\mu m * 100\mu m$ |
| Power efficiency | 60% |
| Voltage conversion efficiency | 90.9% |
| BGR: | |
| Area | $230\mu m * 230\mu m$ |
| Supply Voltage | $> 1.9V$ |
| PSRR | $-90dB@ < 30KHz/ - 60dB@100KHz$ |
| Power consumption | $61\mu W$ |
| Output Voltage | $1.16V$ |
| LDO: | |
| Area | $100\mu m * 50\mu m$ |
| Respond time | $234ns$ |
| Power consumption | $23\mu W$ |
| Dapper: | |
| Area | $200\mu m * 110\mu m$ |
| INR | $1.7\mu V$ |
| Signal mixing technique | DFF |
| Supply Voltage | 1.4V |
| Power Consumption | $11\mu W$ |
| Amperometric Input Current Range | $80pA - 1\mu A$ |
| Amperometric output frequency | $210Hz - 1.3MHz$ |
| Potentiometric Input Voltage Range | $0V - 1V$ |
| Potentiometric output frequency | $9.014Hz - 1.366Hz$ |

## 7.2 Future Work

The future work will be considered in two ways: performance optimisation and redesign of the WPDT to be able to supply different front end sensor.

Several blocks can be optimised. Most of the transistors and the capacitors in the BGR are able to minimised further to decrease the area occupation.The PSRR can be

further improved at the high frequency band. The resistor divider in the LDO circuit can be replaced by higher resistive ones to decrease the quiescent power consumption. And a low power buffer can be placed between the WPDT and Dapper to achieve a more stable system. How to redesign the Dapper system so that it can be used in more applications is also worth considering. The boundary between amperometric frequency and potentiometric frequency should also be paid attention. If the amperometric frequency is too low or potentiometric frequency is too high, the mixed signal can not tell the difference and these two separate information can no longer be recovered. This Dapper can not only measure the pH and glucose if the front end is replaced by other sensor. Thus a large range of voltage input and current input is desired to fits in more general applications.

The WPDT system can be redesigned to have different states controlled by the RF signal so that it can power different supply level front end sensor, not only the $1.4V$ system. It can also be redesigned to have low power mode and fast operation mode. It can even to be able to store the excess power to increase the power efficiency.

Due to the Covid-19, The university laboratory is closed and the prototype can not be implemented and tested. In the future, this body dust system should be tested and measured in the laboratory practically.

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# Appendix A

# Schematics

The schematics here shows the schematics of each circuit block.

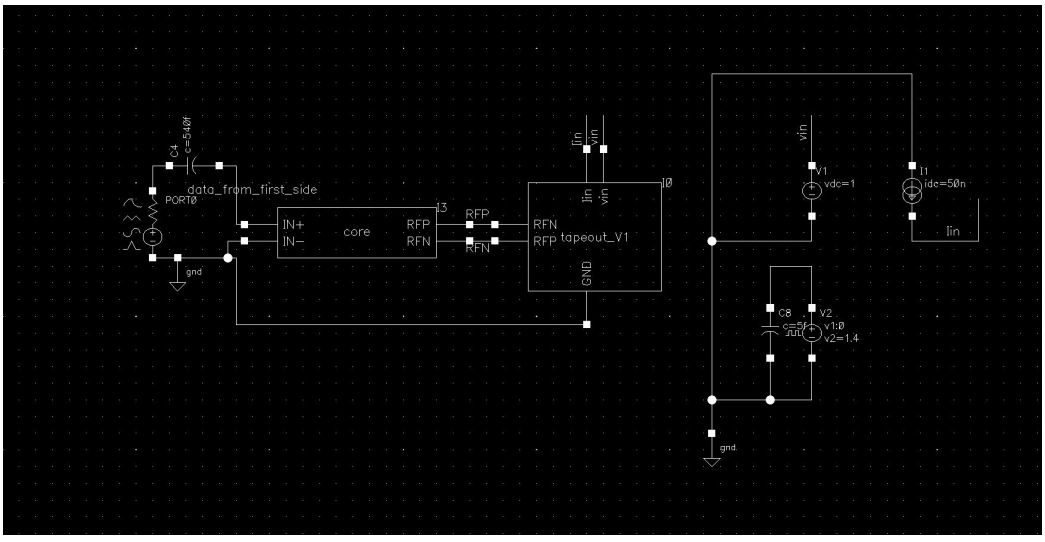


Figure A.1: The diagram of system test bench

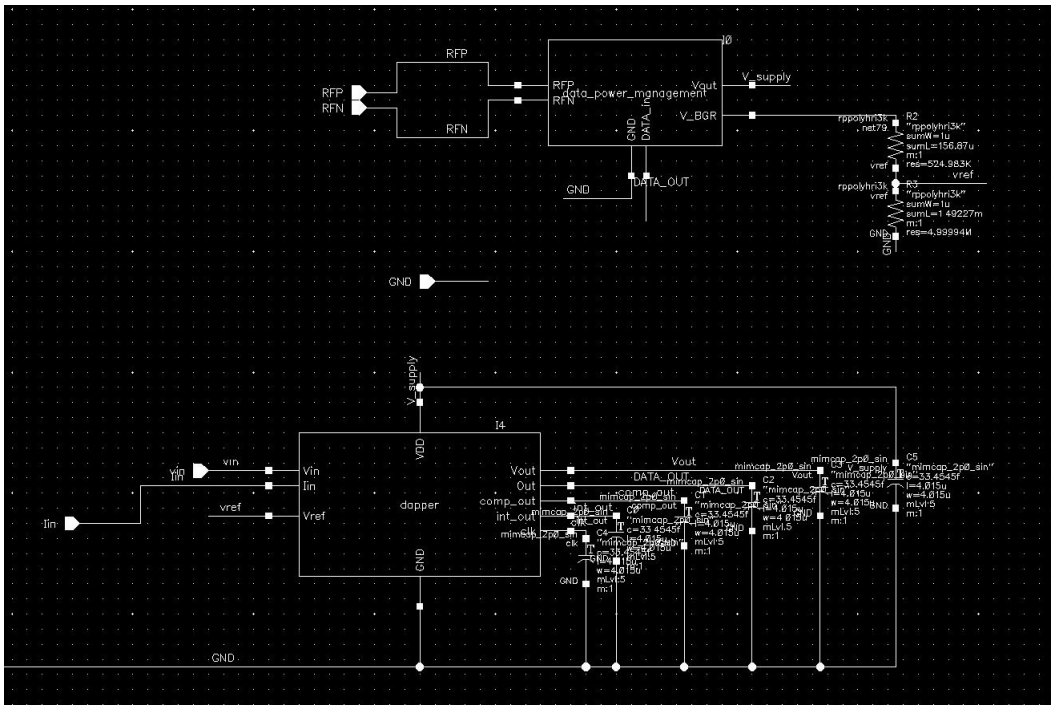


Figure A.2: The diagram of body dust top level interconnection

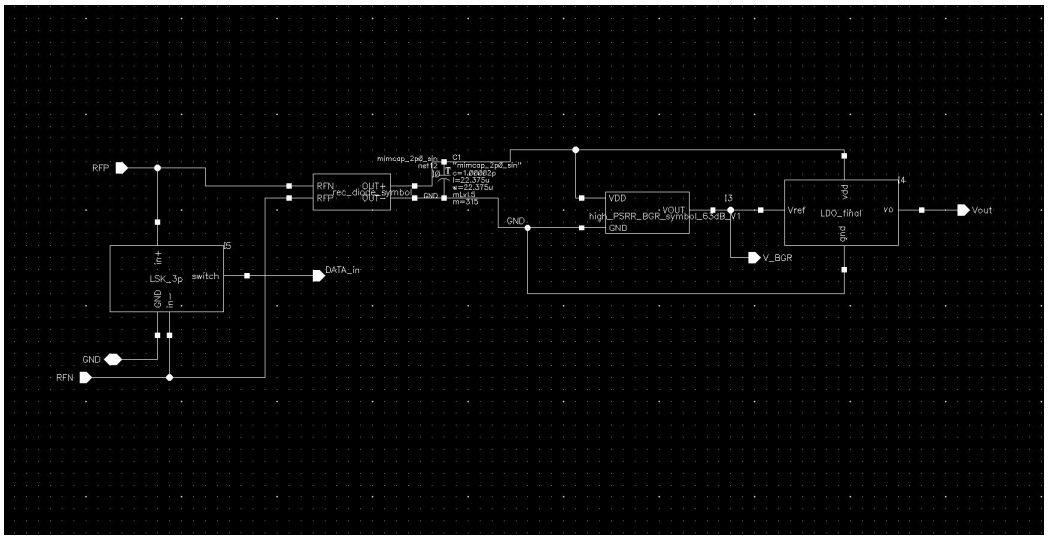


Figure A.3: The diagram of WPDT system

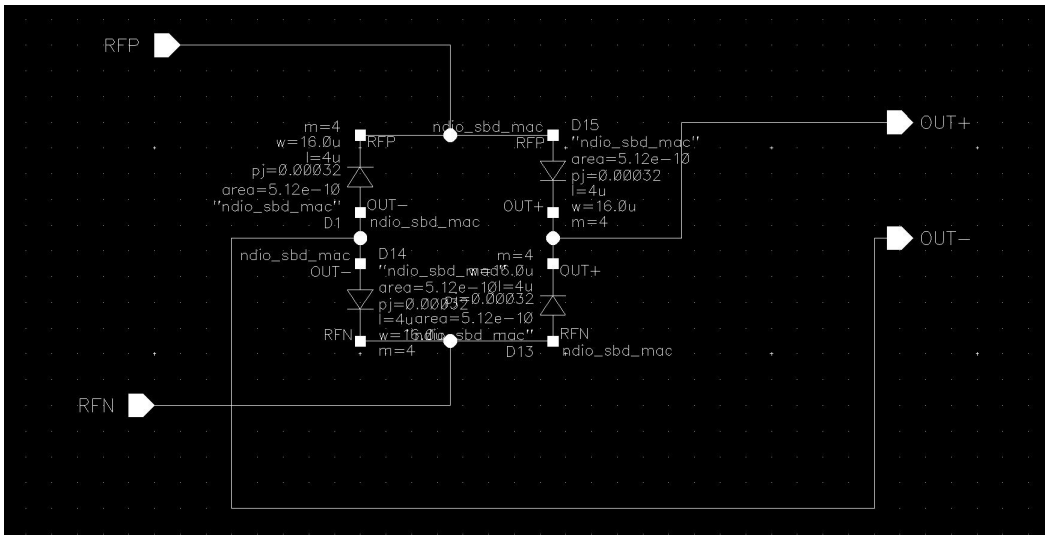


Figure A.4: The diagram of rectifier

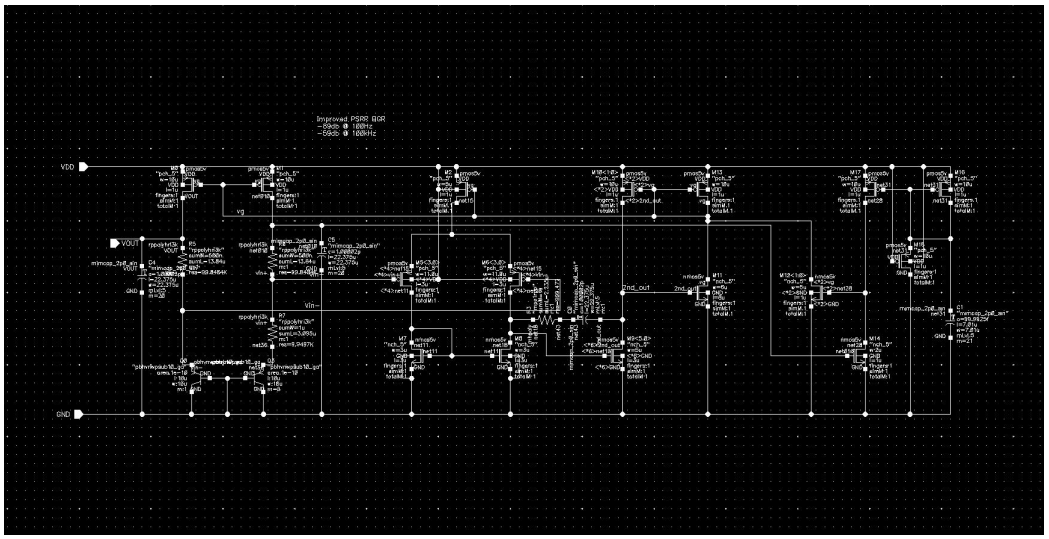

Figure A.5: The diagram of band gap reference

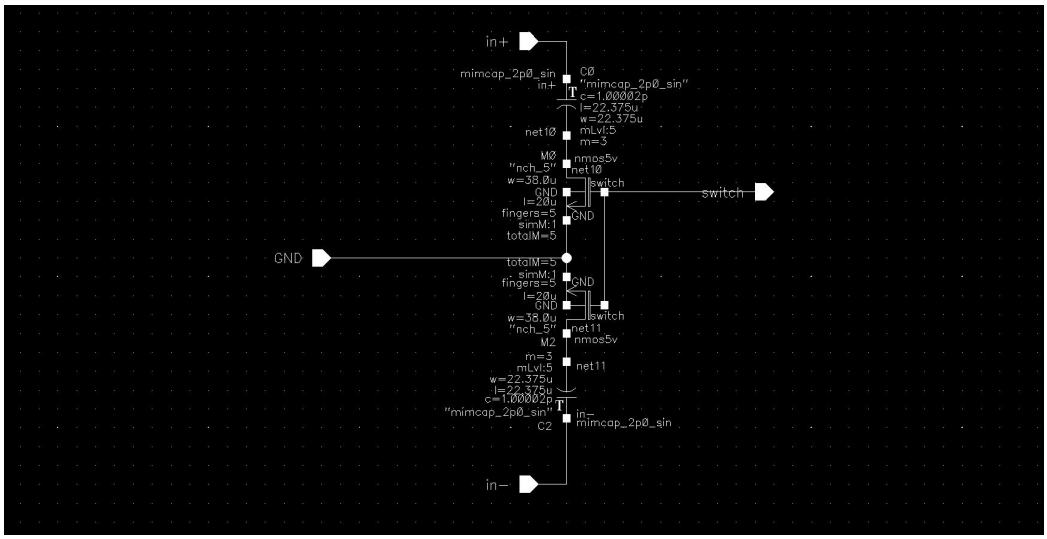


Figure A.6: The diagram of load shift keying

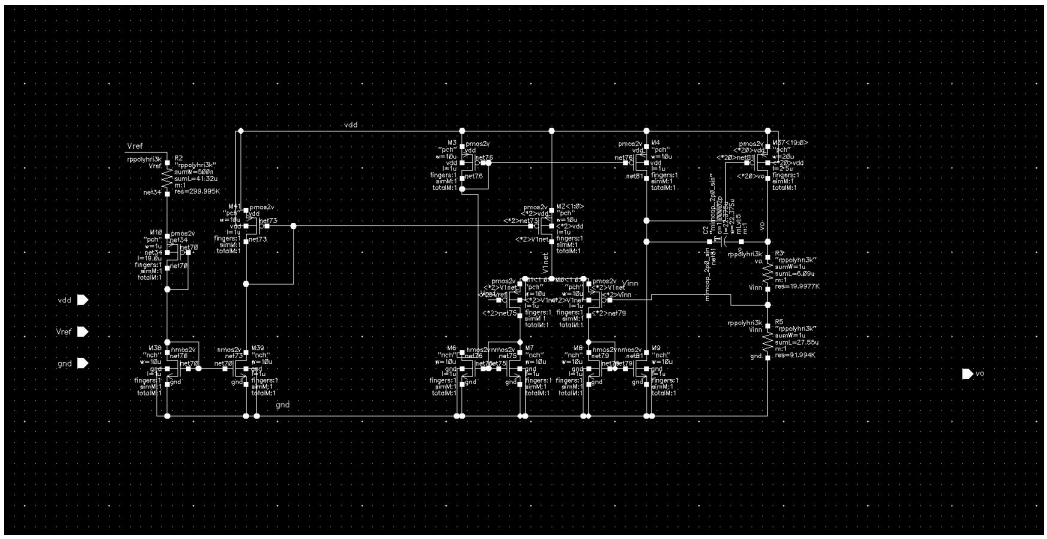


Figure A.7: The diagram of low drop out circuit

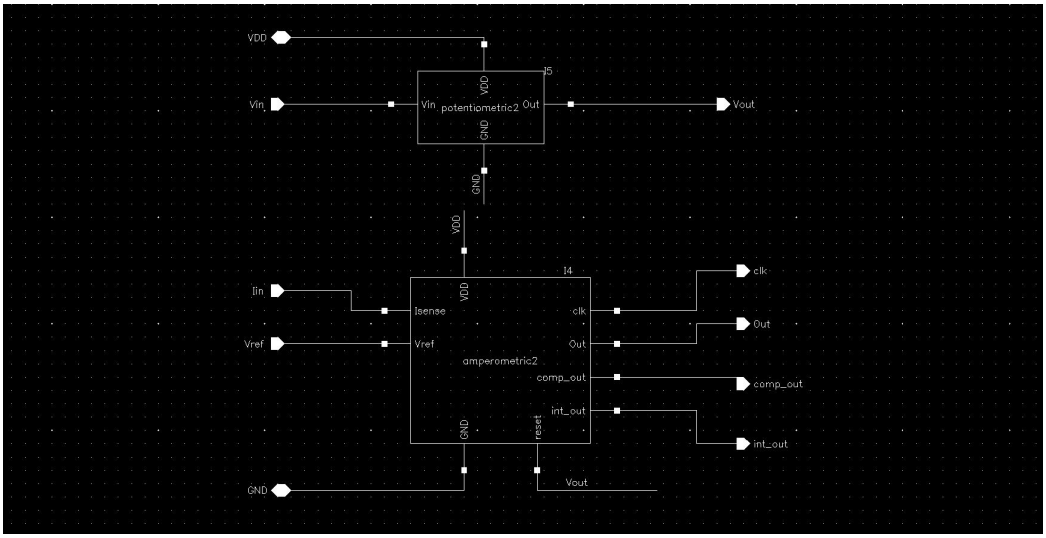


Figure A.8: The diagram of front end dapper

# Appendix B

# Publication extracted from this work

The publication extracted from this work will be submitted to the conference IEEE ISCAS 2021, and is attached here:

# Body Dust: A Wireless Data and Power transmission system for Electro-Chemical Front End Sensor

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***Abstract*—In this work, A low power Wireless Electro-chemical Sensor system is presented. Due to its nature of small size and low power-consumption, not only can it be used as implanted biomedical applications, but also in some out-body systems. The proposed systems optimized the conventional slew-rate detection low drop out (LDO) circuits by using a self-tuned structure, reducing the respond time to 100ns. The static power required for this LDO reduces to 2µW. Due to the nature that back-telemetry technique load shift keying (LSK) can cause power supply ripple, a high PSRR Band Gap Reference (BGR) is applied, achieving a PSRR of 60dB at 100kHz, with an output reference voltage deviation of 1mV. The RF power is transmitted at 433MHz with a backscattering data rate up to 300kHz. The internal power management circuit provides a 1.4 stable DC supply for the front end Electro-chemical Sensor with a power consumption of 100µW.**

***Keywords*— *Wireless Power Transfer, LSK, LDO, BGR, low power***

## I. INTRODUCTION

Given the interest in wireless power transfer (WPT) technology over the past years, many areas have been further developed owing to the advancement of WPT. Besides some traditional applications such as cellular phone, laptop and electronic vehicles, biomedical devices also benefit from building a wireless connection between humans' body and external circuits [3]. Power transfer from out-body circuit to in-body system is the pre-requisite for implanted devices, and the demands for recharging battery, even replacing the implanted component, no longer exist. As a result, no invasive battery wires are needed and the lifetime of the applications is not limited by the small volume battery.

Amongst all the biomedical devices, growth and advances of electrochemical sensing have fulfilled and progressively elevated several areas for its sensitivities to specific analytes and possibility of real-time biofluids sensing [5]. An important biomolecule used for medical purpose is glucose, however, glucose detection could be challengingdue to the environment variability, such as biofluids pH. The detection of targeted biomolecules is consequently acquired by calibration of environment fluid pH. Thus, real-time and concurrent amperometric and potentiometric detection is necessary for these two different analytes.

This paper presents a low power implanted wireless electrochemical sensor system, based on a dual amperometric and potentiometric power efficient instrumentation (Dapper) sensor[5]. The data detected by the sensor is transferred wirelessly through the inductive coils by load shift keying (LSK). But the LSK will also cause the voltage ripple at second side coil, thus affecting the supply voltage for front end sensor. The proposed system utilized an autonomous self-tuned LDO to mitigate the voltage fluctuation from previous stages. For the purpose of low power consumption and simple structure, upload circuit is not required with a power on reset circuit. The front-end dapper sensor consumes 11µW from 1.4V supply and performs a 0V -1V potentiometry and 80pA - 1µA amperometry range [5]. The output frequency is up to 300kHz at the maximum sensing current. The entire body dust system consumes 100µW power.

The rest of this paper is organized as follows: the section II introduces operational principle of the system and demonstrates the novelty of this architecture. Section 3 details the circuit implementation. Section 4 illustrates the simulation results. Section 5 concludes this work.

## II. SYSTEM ACHITECTURE

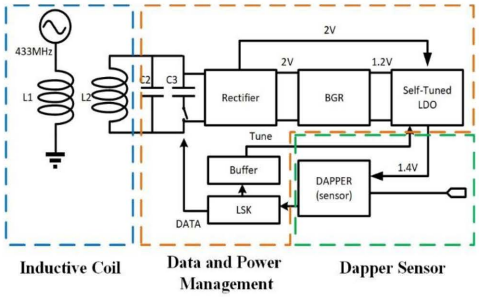


*Figure 1 Body dust system architecture*

The integrated Body dust system is shown in the Figure 1. The inductive coils are designed and manufactured at a working frequency of 433MHz with a maximum PTE of 19.2% [6], which leaves sufficient bandwidth for future multiple channel systems. The second coil receives RF power from the extern circuit and feeds this AC power to a bulk-regulated rectifier, where the AC voltage will be converted to a DC supply with a smoothing capacitor. A high PSRR Band Gap Reference, following the rectifier, is responsible for providing a stable 1.16 reference voltage for the self-tuned Low Drop Out (LDO) circuit, which is capable of down-converting the 2V DC supply to a regulated 1.4 voltage supply for Dapper sensor.

The sensor performs real-time sensing and concurrent potentiometry and amperometry measurement, generating a single square wave output combining a high frequency amperometry signal and low frequency potentiometry signal. The data is transmitted through an LSK by switching in or out a parallel capacitor C3 to tune the LC tank resonant frequency. This frequency shift is reflected to the external

coil with a voltage change across the coil [7]. Thus, the sensor signal is able to be recovered at the external circuit.

However, a voltage fluctuation can also be observed at the second coil due to the LSK, deteriorating the stability of BGR and LDO. This voltage fluctuation can be mitigated by using a large value capacitor at a cost of a large area. Besides, a high PSRR BGR is required in this case to provide stable reference voltage. A novel self-tuned LDO is also proposed in this work to minimize its input voltage fluctuation and reduce the power consumption.

## III. CIRCUIT IMPLEMENTATION

The Body dust prototype is developed using TSMC180 technology, and each circuit block is detailed below.

### A. Bulk Regulated Rectifier

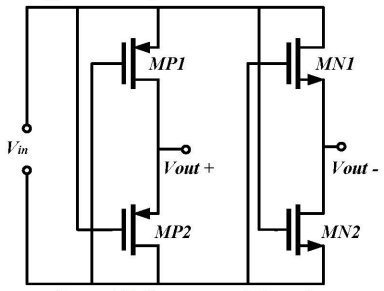


*Figure 2 Fully cross-coupled rectifier*

A rectifier converts the received AC power to the DC power which can be used as power supply by the internal circuit. The convetional rectifiers are usually implemented by diodes, which are not suited in CMOS process [3]. In this work, the rectifier is fullfilled using a fully cross-coupled rectifier,where the transistors at two branchs are cross coupled, shown in Figure 2. The principle of this rectifier is that in each half cycle of the circuit, either MN1 and MP2 or MP1 and MN2 are turned on, forcing the output node Vout+ always higher than Vout-. This circuit has an advantage of low voltage drop, thus a high voltage convernsion ratio. This voltage drop is now due to two transistors' drain-source voltage instead of two threshould voltage of diodes in convetional rectifier architecture.

$$V_{loss} = V_n + V_p = \sqrt{\frac{2I_d L_n}{\mu C_{ox} W_n}} + \sqrt{\frac{2I_d L_p}{\mu C_{ox} W_p}} \approx 0.4V$$

However, this rectifier shows a low power converntion effciency (PCE) due to the possibility of flow back current, achieving a maximun PCE of 60% at working frequency of 433MHz [6].

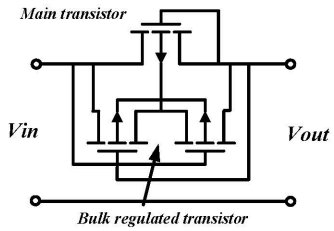


*Figure 3 Bulk regulated circuit*

For mitigating the body effect, the bulk of each transistor is supposed to be always connected to its source. Thus, a bulk regulated circuit is applied to each transistor, shown in Figure 3, at a cost of the increased area. This circuit works such that among the two bulk regulated transistors, only the one which connects to the lower voltage potential is turned on, ensuring the main transisor's bulk is connected to its lower potential side.

### B. High PSRR Band Gap Referrence

A bandgap reference can be achieved by combining the CTAT behaviour of a diode's forward voltage drop and the PTAT behaviour of the thermal voltage from a BJT [8]. A conventional BGR is formed by using a PTAT current generated from base-emitter junctions of BJT with the help of an opamp to fix potentials to give a PTAT voltage drop (across resistors) and a CTAT voltage drop (across diodes). This kind of conventional BGR has a low Power supply rejection ratio, which is an important characteristic in this system due to the supply fluctuation caused by the LSK. According to [6] (3)

$$PSR = \frac{v_{ref}}{v_{dd}} \propto \frac{1 - PSR_{opamp}}{A}$$

Where $PSR_{opamp}$ is the PSR of the Opamp used in the BGR and $A$ is the gain of Opamp. It can be noted that if the opamp follows the change of power supply, the PSRR of the BGR is infinity. Thus, a high PSRR BGR is applied to this system, shown in Figure 4.

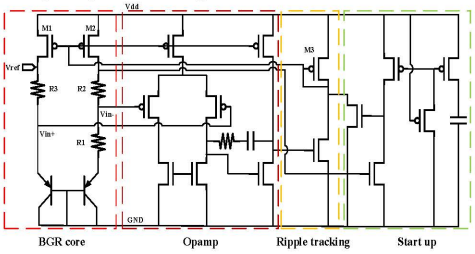


*Figure 4 High-PSRR BGR schematic*

This circuit is composed of four parts. The bandgap core provides a temperature independent voltage output by combining a PTAT and a CTAT voltage:

$$V_{out} = V_{be1} + \frac{R_2}{R_1} V_T \ln(8) \approx 1.2V$$

The Opamp forces its two input nodes *Vin+* and *Vin-* at a same potential level, ensuring the current flowing through R1 is fixed, as well as current flowing through R3 by the current mirror M1 and M2. A supply ripple tracking circuit is added after the Opamp. A PMOS M11 is diode-connected in series with a common-source NMOS, feeding the ripple of input supply at its source side direct to its drain and gate sides, which is the output stage of the Opamp. Thus, the output of this Opamp could track the ripple of supply, thus fixing the source-gate voltage of the M1 and M2. If M1 and M2 are long channel length Pmos, the channel length modulation is neglected, thus their *Vds* will not affect the drain current. As a result, the current flows through M1 and M2 are always fixed regardless of the power supply ripple. A start-up circuit is attached to this circuit, enabling M1 and M2 working at the saturation

region during the power on stage, reducing the settle time. The PSRR of this BGR achieves at -86dB at 10kHz and -60dB at 100kHz.

### C. Load Shift Keying

There are different strategies to transfer wireless power and data. The easiest way is to use two different coils – one for power transmission and the other for data transferring. However, this technique is not suitable for biomedical applications which require low power and small size circuits. An LSK, which is a wireless communication scheme having some advantages over frequency shift keying and phase shift keying, provides a simple and low power circuit architecture, and also allows single coil transmission for data and power at the same time.

An LSK usually modulates the series inductors or parallel capacitance at the second side coil to shift the resonant frequency of the RF power link [7]. This shift is reflected back to the primacy side and can be observed as a voltage change across the primary coil. However, this resonant frequency shift may cause the decrease in power transmission efficiency, which can be mitigated by calculating the proper value of switching parallel capacitance.

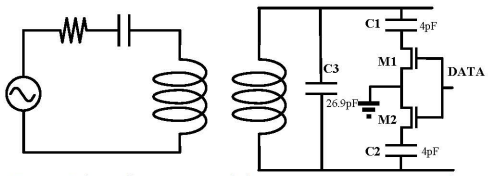


*Figure 5 A wireless power and data transmission system with a LSK circuit*

Figure 5 shows the schematic of an LSK circuit. In order to strongly switch on the NMOS switch M1 and M2, two parallel capacitors are connected in series. Considering the parasitic capacitance of the M1 and M2, the size of M1 and M2 should be large enough to shift the resonant frequency by a sufficient amount. For the purpose of maintain the highest PTE, C1 and C2 are set to 4pF. As a result, the voltage shift across the primary coil is 200mV, large enough to recover the data information.

### D. Self-Tune Low Drop Out circuit

A Low drop out (LDO) circuit is becoming more important in power management circuits especially in biomedical applications. It can convert the supply to a relative low level to minimizing the system power consumption. However, conventional LDO circuits suffer from slow respond time, slow slew rate and low bandwidth. Recently, many techniques are proposed to improve these flaws [7-9]. Mostly of them utilizing slewing detection from internal node to boost the current as the input voltage changes. But these are not suitable for systems if the input voltage only changes by a small amount, since it will hardly be detected. A new self-tuned LDOs is proposed in this work to work with a 50mV input ripple from the rectifier circuit, shown in Figure 6

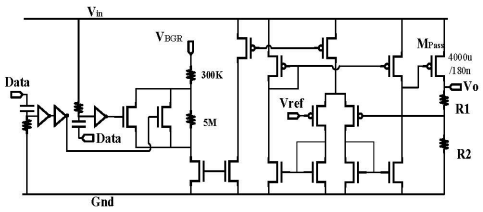


*Figure 6 the proposed self-tuned LDO circuit*

The working principle of this circuit is that the LDO boosts its working current while the Vin changes. Since in this system, Vin of this LDO is the output voltage from the rectifier with a ripple around 50mV due to the LSK. This digitized data from the sensor driving the LSK can also be used to tune the LDO circuit. The digitized data is connected to a high pass Capacitor-resistor circuit to trigger the buffer only at the edge of the data signal, in order to decrease power consumption of the steady stage. With the help of delay buffers, the working current of the opamp can be boosted, thus the respond time and the slew rate are improved.

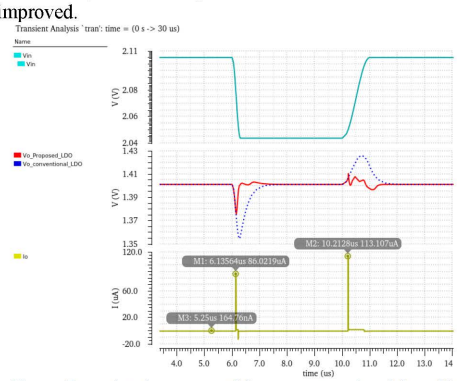


*Figure 7 simulated response of the conventional and the self-tuned LDO circuit.*

Figure 7 demonstrates the simulated results of the conventional and proposed LDO circuits. As the Vin changes from 2.11V to 2.04V, the static current boosts to 86uA from 164nA, dramatically reducing the respond time, from 1.5us (blue dot line) to 100nS (red solid line). Due to the large smoothing capacitor after the rectifier, it takes Vin 1us to change from 2.04 to 2.11V, increasing the LDO respond time as well. The proposed LDO reduces the ripple from 20mV to 5mV and also decreases the respond time.

### E. Dapper sensor

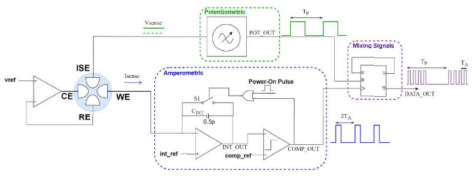


*Figure 8 Dual amperometric and potentiometric sensor [5]*

Figure 8 demonstrates the structure of the front-end sensor in this system [5]. It uses the ion-selective property of ISFET and mixes the amperometric signal, generated by a capacitor integrated and a comparator, and the potentiometric signal, generated by a voltage-controlled oscillator. The entire sensor circuit consumes 11 µW at a 1.4V supply. The measuring range of this sensor is 0V – 1V and 80pA to 100µA, generating a mixed square wave with a frequency from 1Hz to 300kHz. The input referred noise is 1.7µV and 44.6µA.

Figure 9 shows the system layout diagram of the body dust system. The whole system occupies 936µm*426µm area.

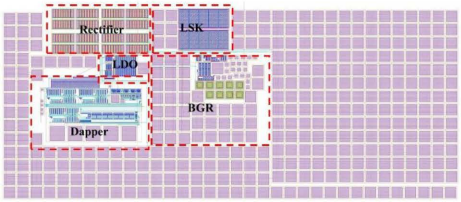


*Figure 9 System Layout diagram*

## IV. Measured Redults

The circuit was designed and will be fabricated using the TSMC 180 um technology. The circuit area is estimated to be 3um*3um, constrained by the coils size. The transient response of the system is shown in the Figure 10.

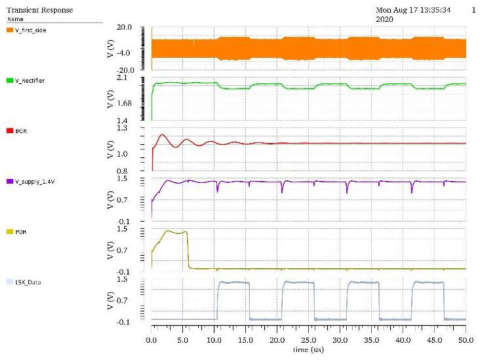


*Figure 10 transient simulation of the body dust system*

The $I_{sense}$ and $V_{sense}$ of the system are set to be 25nA and 900mV in this simulation. The Data frequency generated by DAPPER achieves 300kHz. The voltage shift detected at the primary side is about 1V, large enough to be recovered. The ripple of the supply from rectifier is around 50mV, while there is only 1mV fluctuation of BGR.

The maximum efficiency of the rectifier can be achieved at 60% when the W/L of the transistors are set to be 18/1 and the RF input power is 14dBm [6]. The designed BGR consumes a static power of 60uW and generated an output reference voltage of 1.16V with a deviation of 1mV at 300kHz. The PSRR of this BGR as a function of frequency is shown in Figure 11. The PSRR achieves more than 85dB below 10kHz while reducing to 60dB at 100kHz.

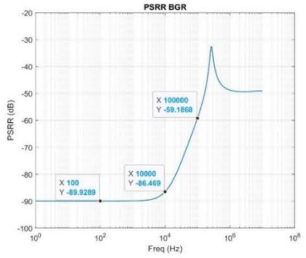


*Figure 11 simulated PSRR of the BGR in this work*

The designed LDO consumes only 2µW static power and has a respond time less than 100ns, providing a stable 1.4V for the Dapper sensor. In order to allow the maximum slew rate. The size of pass transistor in the LDO is set to be 4000µ/180n.

TABLE I
SYSTEM CHARACTERISTICS AND COMPARISON WITH STATE-OF-THE-ART

| Parameter | | This work | [1] | [2] | [4] |
|---|---|---|---|---|---|
| *Year* | | 2020 | 2019 | 2018 | 2018 |
| *Application* | | LSK | LSK | LSK | LSK |
| *Tech* | *[nm]* | 180 | PCB | 180 | 350 |
| *RF frequency* | *[Hz]* | 433M | 1.93M | 13.56M | 433M |
| *Supply-V* | *[V]* | 1.4V | 3.5-4 | 2-3 | 1.5 |
| *Core-A* | *[mm²]* | 9 | 28 | 25 | 2.1 |
| *Data Bandwidth* | *[Hz]* | 300k | 10k | 211k | 825 |
| *INR* | *[µV]* | 1.7 | N.A | 2.09 | 1.8 |
| *Power Dissipation* | *[W]* | 100 µ | 44m | 3.12 | 92µ |

## V. Conslusion

This work demonstrates a low power self-tuned wireless electro Electrochemical Sensor system. Due to its nature of small size and low power, it can be used in many aspects such as in implanted devices or in Internet of things systems. With the help of the LSK, the data generated by the sensor can be easily recovered at the primary side coil. A self-tuned LDO circuit is proposed to simplify the conventional slew rate detection LDOs and increase its slew rate as well. The overall system power budget is estimated to be 100 µW and can be further improved by reducing the power of BGR if the PSRR constraints of BGR is not very high. The RF power is transmitted at 433MHz for a maximum transmission efficiency and the back-telemetry data rate can achieve 300kHz.

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