2021 IEEE International Symposium on Medical Measurements and Applications (MeMeA) | 978-1-6654-1914-7/20/$31.00 ©2021 IEEE | DOI: 10.1109/MeMeA52024.2021.9478690

Design of Low-Power Highly Accurate CMOS Potentiostat Using the $\mathbf{g_m/I_D}$ Methodology

Yaohua Zhang*, Daryl Ma*, Sandro Carrara† and Pantelis Georgiou*
*Department of Electrical and Electronic Engineering, Imperial College London, UK
†Integrated Systems Laboratory, EPFL, Switzerland
Email: *yaohua.zhang16@imperial.ac.uk, *jianwen.ma13@imperial.ac.uk, †sandro.carrara@epfl.ch, *pantelis@imperial.ac.uk

***Abstract*—This paper presents the design of CMOS potentiostats using the $\mathbf{g_m/I_D}$ methodology. We investigate the $\mathbf{g_m/I_D}$ methodology as a systematic framework for optimal potentiostat design in terms of power dissipation, noise and area, the three most important potentiostat performance criteria. To this end, we select a reference potentiostat design and redesign this reference circuit using the $\mathbf{g_m/I_D}$ methodology in a 0.18 μm CMOS technology. Simulated results show that the power dissipation can be reduced by using the $\mathbf{g_m/I_D}$ methodology. For instance, the power dissipation of the folded cascode op-amp decreased from from 409.641 nW to 161.674 nW, indicating a 60.5% improvement. The total transistor occupation area of the folded cascode op-amp also decreased from 307 μm^2 to 275 μm^2, indicating a 10.4% improvement. We demonstrate that the $\mathbf{g_m/I_D}$ methodology is a good tool for analogue IC design as it can help the designer understand performance trade-offs as well as determine transistor dimensions, which can otherwise be very time-consuming.**

***Index Terms*—$\mathbf{g_m/I_D}$ methodology, potentiostat, amperometry, two-stage CMOS op-amp**

I. Introduction

Biosensors that detect and quantify biological analytes play a critical role in many modern clinical research, pharmaceutical, environmental and healthcare applications [1]. Out of the diverse range of biosensors, electrochemical biosensors that convert the detection of the target analyte into the electronic/digital information domain directly have become extremely popular and prevalent. Electrochemical biosensors also possess the advantages of shorter detection time and reduced system complexity as compared to traditional optical sensing techniques that require sample labelling [2]. In addition, the exponential growth in the microelectronics industry as described by Moore's Law has contributed to the upsurge in electrochemical biosensors. CMOS technology has become the perfect candidate for implementing instrumentation functions in biosensors. CMOS ICs form an indispensable part in modern electrochemical biosensors and even in futuristic consumable diagnostic sensors as proposed in the Body Dust project [3].

Having established the significance as well as the ubiquitous presence of CMOS ICs in biosensors, we focus our attention to a key component in CMOS instrumentation circuits – the potentiostat. In essence, a potentiostat is the electronic circuit widely used in three-electrode amperometry systems (the most prevalent form of electrochemical biosensors) that fulfills two basic functions of maintaining a desired potential difference between the working electrode (WE) and reference electrode (RE) and measuring the amount of current directed through the counter electrode (CE) [4]. Some examples of potentiostats can be found in [5]–[10]. The potentiostat is inherently an analogue circuit with many crucial performance trade-offs to consider. For instance, when deployed in a fully implantable application, the potentiostat must satisfy stringent and even conflicting performance targets such as low power dissipation, low noise and small area. As a result, the design of potentiostats is a non-trivial task and as with the design of most analogue ICs is also iterative, time-consuming and heavily knowledge-intensive (experience-dependent) in nature.

In this paper, we apply the g_m/I_D methodology to the design of potentiostats. To the best of our knowledge, this is the first instance of the g_m/I_D methodology being applied to potentiostat design. We demonstrate that on the macro level, the g_m/I_D methodology can provide the designer with clear insights into the fundamental trade-offs in potentiostat design, allowing the designer to make informed and optimal engineering decisions, whereas on the micro level, the g_m/I_D methodology is a practical and time-saving tool that can help the designer size transistors and set bias voltages. In essence, we investigate the g_m/I_D methodology as a systematic framework for optimal potentiostat design in terms of power dissipation, noise and area, the three most important potentiostat performance criteria. To this end, we select the potentiostat circuit proposed in [5] as a reference and redesign this reference circuit using the g_m/I_D methodology in a 0.18 μm CMOS technology. In Section II, we give a brief recap of the the g_m/I_D methodology. In Section III, we explain the g_m/I_D design process of the potentiostat in detail. In Section IV, simulated results are compared to validate our design. Finally, the conclusion is drawn in Section V.

II. g_m/I_D Methodology

The g_m/I_D methodology was first proposed by Silveira, Flandre and Jespers in 1996 [11]. The g_m/I_D methodology was developed in part to address the growing discrepancy between hand-analysis and simulation results in analogue CMOS IC design, as well as to provide a novel, systematic way of designing circuits with a strong grasp of the inherent trade-offs [12].

The central idea of the g_m/I_D methodology is to analyse and design analogue ICs according to the transistor's inversion

978-1-6654-1914-7/21/$31.00 ©2021 IEEE

level, for which the g_m/I_D (transconductance efficiency) figure of merit is a good proxy [12]. Equations 1 and 2 clarify this further.

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{\partial \ln I_D}{\partial V_G} = \frac{\partial \ln[\frac{I_D}{W/L}]}{\partial V_G} \tag{1}$$

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{1}{I_D}\frac{I_D}{nU_T} = \frac{1}{nU_T} \tag{2}$$

g_m/I_D is the slope (first derivative) of the $\ln I_D/V_G$ characteristic and in the weak inversion region, g_m/I_D is given by (2). It is an established fact that g_m/I_D reaches a maximum in the weak inversion region, where the current-voltage relationship is exponential. The maximum possible g_m/I_D is given by $1/U_T \approx 38.46$ S/A, assuming the thermal voltage $U_T \approx 26$ mV. As the transistor is biased toward the strong inversion region, g_m/I_D decreases in value. g_m/I_D greater than 20 S/A corresponds to weak inversion region; g_m/I_D between 20 to 10 S/A corresponds to moderate inversion region; g_m/I_D between 2 to 10 S/A corresponds to strong inversion region [12]. It should also be noted that these ranges of g_m/I_D remain relatively constant across transistor technologies [12]. Therefore, g_m/I_D can be used as a good proxy for the inversion level. It follows naturally that we can study the performance trade-offs in biasing transistors in different inversion regions using the g_m/I_D metric. For instance, biasing a transistor in the strong inversion region (small g_m/I_D value) leads to higher transit frequency f_T, i.e. bandwidth, whereas biasing a transistor in the weak inversion region (large g_m/I_D value) leads to greater gain g_m/g_{ds}. This trade-off can be seen in Fig. 1, which shows the mutually conflicting objectives for a single N-channel transistor configured as an intrinsic gain stage (IGS).

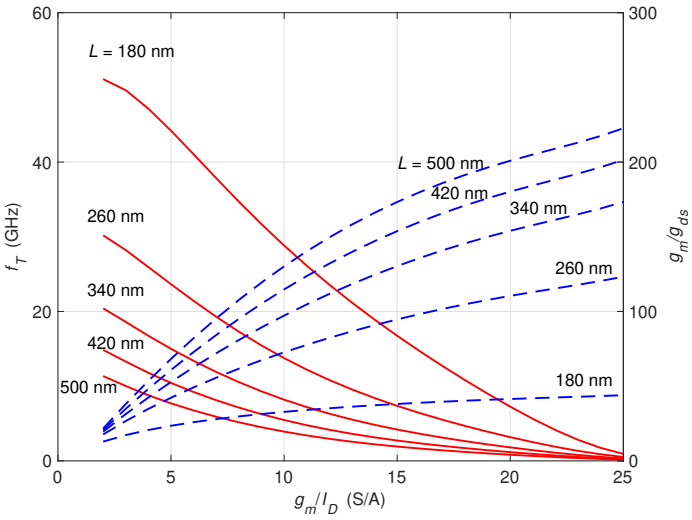

Fig. 1. f_T and g_m/g_{ds} against g_m/I_D for a range of lengths; $V_{DS} = 0.9$ V; $V_{SB} = 0$ V; N-channel IGS in TSMC 180 nm.

In addition, the g_m/I_D methodology also incorporates other fundamental transistor figures of merit such as $g_m/2\pi C_{gg}$ (transit frequency), g_m/g_{ds} (intrinsic gain) and f_{co} (flicker noise corner frequency) in order to study the trade-offs between power dissipation, noise, distortion and bandwidth. A detailed tutorial can be found in [12] but the inherent trade-offs can be summarised as follow. The optimum intrinsic gain, input-referred flicker noise and power dissipation can be achieved by biasing the transistor toward the weak inversion region and setting a long transistor length. However, the intrinsic transistor bandwidth (f_T) is optimised under the opposite conditions of biasing the transistor toward the strong inversion region and setting a short transistor length. This understanding of the inherent performance trade-offs from a g_m/I_D-perspective forms the basis of our potentiostat design methodology, as explained in Section III.

It is also important to note that g_m/I_D is (to the first-order) independent of the width as given in (1), which makes it useful for device sizing. g_m/I_D can be employed to find the widths of transistors in moderate and strong inversion regions by following this procedure elaborated in [12]: i) Derive g_m from the design specifications, ii) Select the transistor lengths to satisfy g_m, speed, area and matching requirements, iii) Decide on g_m/I_D, taking the relevant trade-offs into consideration, iv) Determine I_D/W from g_m/I_D, v) Derive $I_D = g_m/\left(g_m/I_D\right)$, vi) Derive $W = I_D/\left(I_D/W\right)$

The g_m/I_D-centric sizing procedure applies to most high-performance circuits, however, it must be slightly modified when designing low-power circuits biased in the weak inversion region. This is because it is well-known that g_m/I_D is approximately constant in the weak inversion region and as a result, many different designs will be mapped to nearly the same g_m/I_D. In other words, a small error in g_m/I_D could lead to a design that is completely off-target. In this case, the g_m/I_D-centric sizing procedure will have to be modified into a J_D-centric sizing procedure, in which the current density ($J_D = I_D/W$) is used as the design variable [12].

III. g_m/I_D Design Process for Potentiostat

The novel potentiostat topology proposed in [5] and shown in Fig. 2 boasts low power dissipation and high accuracy. It was selected as a reference topology for redesign using the g_m/I_D methodology. In this potentiostat topology, the op-amp A1 is bulk-driven which allows for operation using a low supply voltage (V_{DD} is 1 V) and a low input common-mode voltage level (0.4 V assuming 0.6 V cell potential for glucose detection). This topology also achieves high accuracy, i.e. good matching between the sensor current and the mirrored sensor current using a wide-swing cascode current mirror and the op-amp A2 [5]. A2 serves two purposes. Firstly, it acts as a transimpedance amplifier to produce a voltage output. Secondly, it helps to keep the drain voltages of M1 and M2 identical via negative feedback, ensuring good accuracy between the sensor current and its copy [5].

We begin the g_m/I_D design process for A2 (two-stage op-amp) in Fig. 3 by reminding ourselves of the desirable attributes that this op-amp should possess. The two-stage op-amp should have low power dissipation, small area and low

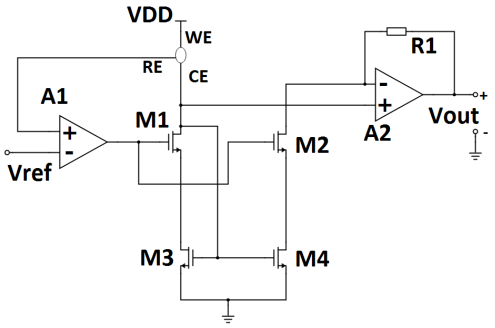

Fig. 2. Reference potentiostat topology, adapted from [5, Fig. 2].

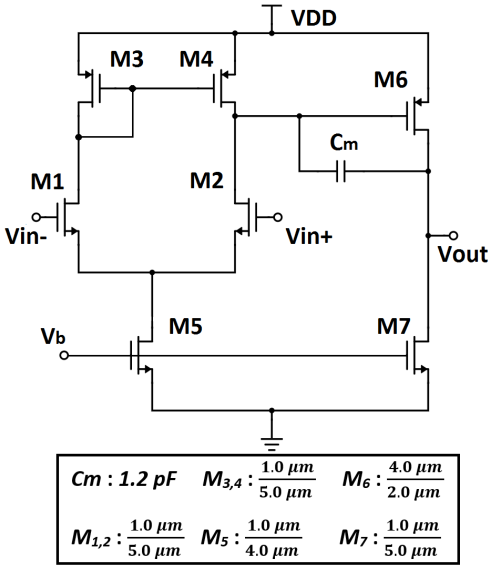

Fig. 3. Two-stage op-amp A2 with transistor dimensions, adapted from [5, Fig. 4b].

noise. In our design, the approach adopted was to bias transistors in a mix of weak and moderate inversion regions. As explained in Section II, the performance trade-offs in analogue circuits such as potentiostats can be largely viewed from the perspective of a transistor's inversion level (g_m/I_D acts as a proxy). Placing transistors in the strong inversion region would lead to greater speed performance, which is not the crucial bottleneck for most implantable contexts. Furthermore, biasing transistors in the strong inversion would leave the designer with hardly any breathing room when optimising for other attributes like power dissipation and flicker noise. On the other hand, by placing transistors in a mix of weak and moderate inversion regions, the designer can optimise for gain, flicker noise and power dissipation. For the transistors that are biased in the moderate inversion region, the g_m/I_D sizing procedure mentioned in Section II is viable. However, for transistors that will be biased in the weak inversion region, the J_D-centric design procedure must be applied instead. In this design, a transistor with a g_m/I_D that is 19 S/A and above is considered to be in the weak inversion region. The J_D-centric

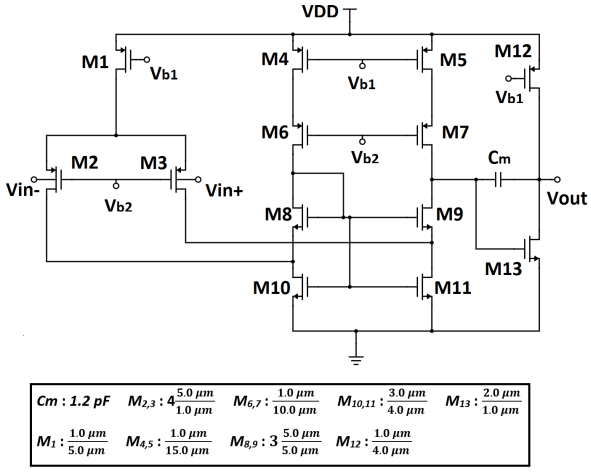

Fig. 4. Folded cascode op-amp A1 with transistor dimensions, adapted from [5, Fig. 4a].

design procedure as elaborated in [12] is i) derive g_m from the design specifications, ii) select the transistor lengths to satisfy g_m, speed, area and matching requirements, iii) decide on $J_D = I_D/W$ for the transistors to be biased in the weak inversion region, iv) determine g_m/I_D from J_D, v) derive $I_D = g_m/\left(g_m/I_D\right)$, vi) derive $W = I_D/\left(I_D/W\right)$.

Moving on with the g_m/I_D design process of the two-stage op-amp, we need to first derive g_m from the design specifications. g_{m2} can be derived from the unity gain frequency (UGF) specification as seen in (3), which assumes that the two-stage op-amp can be approximated as a first-order system under the dominant pole condition. g_{m6} is largely dependent on g_{m2} and is set to be 10 times g_{m2} for stability reasons [13]. In our context of pushing the circuit toward low power dissipation, the UGF of the two-stage op-amp is likely to be very low, e.g. kHz range.

$$f_u \approx \frac{g_{m2}}{2\pi C_m} \tag{3}$$

Subsequently, the design variables to decide upon are the lengths of the transistors. On closer inspection, there are only five unique pairs of transistor widths and lengths to be determined since the current mirror and differential input stage are comprised of matched transistors. It is not always straightforward to decide on the lengths since there are many trade-offs. Therefore, the choice of lengths should be guided by the application context of the circuit and would require some trial and error by the designer. The lengths decided on can be seen in Fig. 3.

Next, the most important step of this design procedure is to determine the g_m/I_D or J_D of the transistors. It is undeniable that the two most important transistors with wide-reaching influence are M2 and M6, the differential input transistor and the second stage P-type common source amplifier respectively. In order to push down power dissipation, at the expense of

bandwidth, M2 and M6 are biased in the weak inversion region. On the other hand, the current mirror transistors (M3 and M4), current source transistors (M5 and M7) are secondary and are biased in the moderate inversion as a compromise. In our design, $(J_D)_2 = 28.618 \times 10^{-9}$ A/μm, $(J_D)_6 = 56.646 \times 10^{-9}$ A/μm, $(g_m/I_D)_{3,4} = 18.5$ S/A, $(g_m/I_D)_5 = 10$ S/A and $(g_m/I_D)_7 = 14.5$ S/A.

Having determined g_m/I_D and J_D, the sizing of the two-stage op-amp is essentially finished. The remaining steps of the sizing procedure (steps iv to vi) are straightforward and can be easily accomplished using MATLAB and SPICE-generated lookup tables [12]. For instance, running a MATLAB sizing procedure for the two-stage op-amp A2 yields the contour plot shown in Fig. 5. The contour plot can help the designer to visualise the pros and cons of his (her) design choices. From Fig. 5, it can be seen that selecting a point with smaller J_{D2} and J_{D6} values, which means placing M2 and M6 in the weak inversion region leads to lower power dissipation. The gain also improves; however, the total transistor area increases. The time spent on this design has been significantly reduced compared to manual tuning. The redesigned transistor dimensions can be seen in Fig. 3.

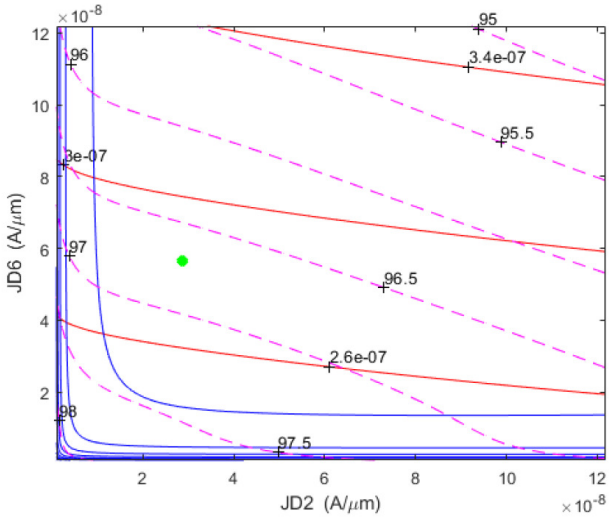

Fig. 5. Optimised design contour curves for two-stage op-amp A2. Total DC current (nW, red), total active area (μm^2, blue), and total gain (dB, dashed magenta) contour curves. The selected point is marked by the green dot.

The g_m/I_D design process of the folded cascode op-amp is very similar. The redesigned transistor dimensions can be seen in Fig. 4, whereas the results can be seen in Table II.

IV. Results and Discussion

The original and redesigned potentiostat circuit were simulated in Cadence Spectre with TSMC 0.18 μm technology. Table I summarises the simulation results as well as the target specifications for the two-stage op-amp redesigned using the g_m/I_D methodology and the original two-stage op-amp in [5]. Similarly, Table II summarises the simulation results as well as the target specifications for the folded cascode op-amp

TABLE I
Simulation results, specifications and percentage improvement for two-stage op-amp A2

	Simulation Results	Specifications	% Improvement
Stage 1 Current (nA)	57.236 (64.159)	≤ 100	-
Stage 2 Current (nA)	226.584 (261.749)	≤ 250	-
VDD (V)	1	1	-
Total Power Dissipation (nW)	283.820 (325.908)	≤ 350	12.9
Stage 1 Gain (dB)	49.794 (49.847)	≥ 40	-
Stage 2 Gain (dB)	47.252 (46.503)	≥ 40	-
Total Gain (dB)	97.046 (96.350)	≥ 80	-
Phase Margin	53.990° (64.007°)	$\geq 45°$	-
UGF (kHz)	70.918 (52.409)	≥ 50	-
Total Transistor Occupation Area (μm^2)	37 (34)	-	-8.82
Total Input-referred Noise (μV, 0.001 Hz - 10 kHz)	21.695 (20.910)	-	-3.75

TABLE II
Simulation results, specifications and percentage improvement for folded cascode op-amp A1

	Simulation Results	Specifications	% Improvement
Stage 1 Current (nA)	92.614 (283.595)	≤ 100	-
Stage 2 Current (nA)	69.060 (126.046)	≤ 250	-
VDD (V)	1	1	-
Total Power Dissipation (nW)	161.674 (409.641)	≤ 350	60.5
Stage 1 Gain (dB)	70.277 (78.028)	≥ 40	-
Stage 2 Gain (dB)	44.890 (-1.638)	≥ 40	-
Total Gain (dB)	115.167 (76.390)	≥ 80	-
Phase Margin	47.680° (49.137°)	$\geq 45°$	-
UGF (kHz)	30.327 (62.202)	≥ 50	-
Total Transistor Occupation Area (μm^2)	275 (307)	-	10.4
Total Input-referred Noise (μV, 0.001 Hz - 10 kHz)	59.555 (31.267)	-	-90.5

redesigned using the g_m/I_D methodology and the original folded cascode op-amp in [5]. The data in round parentheses in Tables 1 and 2 refer to that of the original design in [5], whereas the data without parentheses refer to that of the g_m/I_D-based design.

We can see that the op-amps redesigned using the g_m/I_D methodology satisfy the target specifications and have lower power dissipation at the expense of total transistor occupation area and/or noise compared to the original design.

In order to compare the op-amps based on their power dissipation, input-referred noise and total transistor occupation

area (sum of WL products across all transistors), we propose a new figure of merit (FoM), a weighted Euclidean distance in a 3-D space as given in (4).

$$FoM_i = \sqrt{\left(\frac{P_i}{\sum_i^n P_i}\right)^2 + \left(\frac{N_i}{\sum_i^n N_i}\right)^2 + \left(\frac{A_i}{\sum_i^n A_i}\right)^2} \quad (4)$$

where P, N and A represent the power dissipation, input-referred noise and total transistor occupation area respectively; n is the number of op-amps that are being compared ($n = 2$ in our context); i is the index for the op-amp for which the FoM is being computed. The smaller the FoM is, the better the design. For the two-stage op-amp, the original design has a $FoM = 0.869$, whereas the g_m/I_D-based design has a $FoM = 0.864$. On the other hand, for the folded cascode op-amp, the original design has a $FoM = 0.954$, whereas the g_m/I_D-based design has a $FoM = 0.856$.

Therefore, we can see that the folded cascode op-amp designed using the g_m/I_D methodology has a smaller FoM and is a better design. The FoMs of the two-stage op-amp are roughly equivalent, which suggests both designs are in an optimal neighbourhood of designs. The g_m/I_D methodology can lead the designer to an optimal neighbourhood of designs, however, to arrive at a global optimum point, the g_m/I_D methodology needs to be augmented by optimisation techniques such as geometric programming, bat algorithm etc. Nevertheless, the g_m/I_D methodology can help the designer save a lot of time otherwise spent tuning in the simulation software.

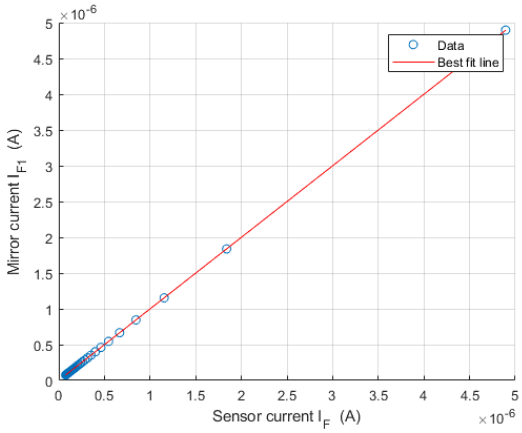

Fig. 6. Simulated linearity of the entire potentiostat optimised with gm/ID methodology.

A linear regression model was implemented in MATLAB. Fig. 6 shows the simulated sensor current and mirrored sensor current in the range of 60.615 nA to 4.895 μA. As shown, the circuit exhibits excellent linearity with a coefficient of determination extremely close to 1.

V. Conclusion

A potentiostat based on the novel topology proposed in [5] was redesigned in TSMC 0.18 μm technology to optimise for power dissipation, input-referred noise and total transistor occupation area using the g_m/I_D methodology. To the best of our knowledge, this is the first instance of the g_m/I_D methodology being applied to the design of potentiostats. The g_m/I_D-based design process offered insights into the trade-offs in the potentiostat circuit to the designer and resulted in less time spent tuning parameters in simulation software.

Acknowledgment

The authors are grateful to Mr Michal Maslik who served as the Cadence system admin and Professor Boris Murmann for his permission to use his g_m/I_D MATLAB code as listed on his website.

References

[1] S. Vigneshvar, C. C. Sudhakumari, B. Senthilkumaran, and H. Prakash, "Recent advances in biosensor technology for potential applications – an overview," *Frontiers in Bioengineering and Biotechnology*, vol. 4, p. 11, 2016. [Online]. Available: https://www.frontiersin.org/article/10.3389/fbioe.2016.00011

[2] H. Li, X. Liu, L. Li, X. Mu, R. Genov, and A. J. Mason, "Cmos electrochemical instrumentation for biosensor microsystems: A review," *Sensors*, vol. 17, no. 1, p. 74, 2017.

[3] S. Carrara and P. Georgiou, "Body dust: Miniaturized highly-integrated low power sensing for remotely powered drinkable cmos bioelectronics," *arXiv preprint arXiv:1805.05840*, 2018.

[4] M. M. Ahmadi and G. A. Jullien, "Current-mirror-based potentiostats for three-electrode amperometric electrochemical sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1339–1348, 2008.

[5] R. Trakoolwattana and A. Thanachayanont, "1-v low-power high-accuracy cmos potentiostat circuit for amperometric sensor," in *2014 11th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON)*. IEEE, 2014, pp. 1–4.

[6] J. Snoeijs, P. Georgiou, and S. Carrara, "Cmos body dust — towards drinkable diagnostics," in *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2017, pp. 1–4.

[7] S. S. Ghoreishizadeh, I. Taurino, G. De Micheli, S. Carrara, and P. Georgiou, "A differential electrochemical readout asic with heterogeneous integration of bio-nano sensors for amperometric sensing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 11, no. 5, pp. 1148–1159, 2017.

[8] D. Ma, S. S. Ghoreishizadeh, and P. Georgiou, "Dapper: A low power, dual amperometric and potentiometric single-channel front end," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.

[9] L. Zuo, S. K. Islam, I. Mahbub, and F. Quaiyum, "A low-power 1-v potentiostat for glucose sensors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 2, pp. 204–208, 2015.

[10] E. Ghodsevali, M. Boukadoum, B. Gosselin, and A. Miled, "Low-power and low-noise fully differential difference amplifier for sub-nanoampere on-chip potentiostat," in *2016 14th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2016, pp. 1–4.

[11] F. Silveira, D. Flandre, and P. G. Jespers, "A g/sub m//i/sub d/based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota," *IEEE journal of solid-state circuits*, vol. 31, no. 9, pp. 1314–1319, 1996.

[12] P. G. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits*. Cambridge University Press, 2017.

[13] P. E. Allen and D. R. Holberg, *CMOS analog circuit design*. Elsevier, 2011.