A Novel Implementation of Concurrent Sensing in Sweat or Blood

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A Thesis submitted in fulfilment of requirements for the degree of
Master of Science
Analogue/Digital Integrated Circuit Design
of Imperial College London

Abstract

Biosensors are essential in detecting diseases and monitoring patients' health status. According to various applications and working scenarios, biosensors could be classified differently. **This project, however, involves in designing one type of biosensors called portable sensors.** Portable sensors gain much attention among researchers due to their capability in **wireless data transmission** and compatibility with **Internet of Things** (IoT).

This report demonstrates the design and simulation of a portable biosensor, which includes a potentiometry, an amperometry, and the circuitry of mixing the above signals together in a single channel. The system has been designed in TSMC180BCD technology with the supply voltage of 1.4V. The characterization of the potentiometry and amperometry includes linearity, input dynamic range, sensitivity, power consumption, area, and noise. The linear dynamic range is **0.3-1V** for potentiometry and **80p-1uA** for amperometry. The maximum power consumption is approximately **16.71uW** when the input voltage is 1V and the input current is 0.5uA.

In addition to the above propsed sensor, an improved version is also introduced in the report. In this improved sensor, the linearity of the potentiometry is better, especially for the low input voltage and the process variation is reduced. Furhtermore, the function of state-transition of the system is achieved by adding two more control bits.

Acknowledgment

Through the journey, several key individuals are vital to this project. Without them and their help, the project could not be possible.

First and foremost, I would like to give my gratitude to my supervisor **Dr. Pantelis Georgiou**, who provides me the opportunity to carry out the project. Thanks for your effort in teaching the lectures, with which I first touched the field of biosensing and learned invaluable knowledge of circuit design.

My appreciation also goes to **Daryl Ma**, who offers me the full guidance throughout the project. Thanks for your patience and effort to check out the progress, arrange the meetings, and answer my questions. Thanks for your encouragement when encountering barriers, thanks for your valuable suggestions and professional aid.

Furthermore, I should also express my acknowledgement to research postgraduate teams in Imperial College Centre for Bio-inspired Technology. Special thanks to **Junming Zeng**, **Miguel Soblechero**, and **Nicolas Moser**, who gave me practical advice on cadence.

I would like to thank my friends and colleagues at Imperial. Thanks for your help and accompany in the whole year, special thanks to **Yiyang Chen** for suggestions in circuit design, **Jiacheng Zhang** for care even in different countries in the last several months.

Finally, I give my special appreciation to my beloved family and fiancee. Their care and encouragement lead me to the completion of the final-year project.

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Abbreviations

TLA:	Three Letter Abbreviation
IoT:	Internet of Things
WSN:	wireless sensor networks
VCO:	voltage-controlled oscillator
DFF:	D-type flip flop
TIA:	transimpedance amplifier
ISE:	Ion-selective electrode
OTA:	operational transconductance amplifier
OA:	Other Abbreviation
COVID-19:	coronavirus diseases 2019
RE:	Reference electrode

Chapter 1

Introduction

1.1 Project Overview

THE coronavirus diseases 2019 (COVID-19) has spread over the world in the last several months. Under the rapid spreading of the epidemic, the scarcity of diagnostics and medical care appears in many countries and regions [3–5]. Additionally, some other diseases, due to lack of diagnosis in the early stage, threaten people's life [6].

Portable sensors might be a possible solution to relieve the above situations. Compared with complex equipment and facilities in the clinic and hospital, portable sensors are cheaper and easier to use. More importantly, with the rise of IoT and the proliferation of smartphones, smartphone-based portable sensors allow for the development of wireless sensor networks (WSN) and mobile health detecting, which could continuously monitor the health status of patients [7, 8]. Patients could also use the detecting results as the preliminary diagnosis of diseases.

This project aims to design a novel portable biosensor that conveys information, like bio-potential and bio-current detected by electrodes in biofluids, into the digital or quasi-digital domain, in which signals are easy to process and are suitable for wireless data transmission. The proposed sensor could mix the signals of the potentiometry and amperometry into a single-channel output, providing a simple interface with wireless platforms.

1.2   High-Level Design

The schematic of the sensor including the interface with the electrodes and power management part is illustrated in Figure 1.1. The electrodes detect PH, ions, or biomolecules in the biological samples (e.g., sweat, blood, urine, saliva, etc.) [8–11] and convert the values and the concentration to the electrical signal, potential and current. Then the proposed sensor senses these signals as its inputs, converts them to a digital or quasi-digital waveform in a single channel, which is easier to read out, transmit, and process. As it is illustrated in the Figure 1.1, the data could be transmitted to smart devices wirelessly.
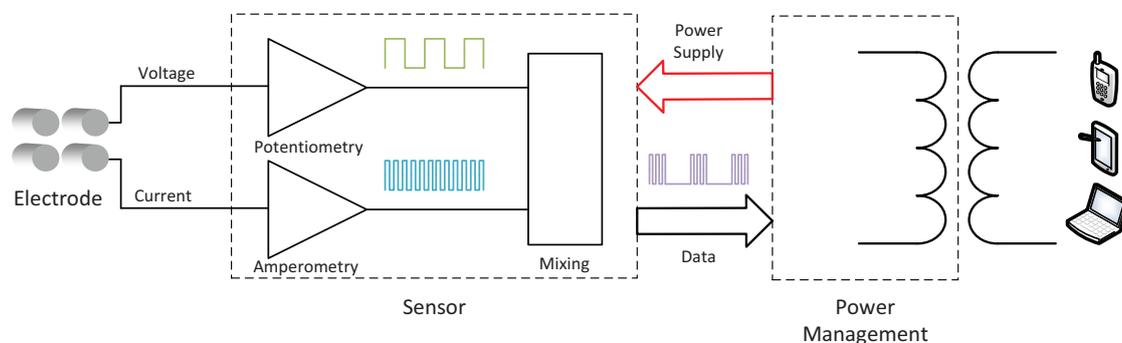
Figure 1.1: The proposed sensor and its interface with eletrodes and power management parts.

1.3   Project Specification

The specification of the proposed sensor is listed in Table 1.1.

1.4   Report Outline

Chapter 2 describes the background of the project, including the definition, classification, and functions of biosensors. The underlying working principles of different biosensors are introduced. This chapter also presents some state-of-art potentiometry and amperometry as well as their specification.

Chapter 3 presents the initial design of the proposed sensor. This chapter begins with the overall structure of the sensor, and then dives into the design of the circuits. The

Table 1.1: General specification of the proposed sensor.

Specification	values
Supply Voltage	1.4V
Linear Range (potentiometry)	0.3-1V (8.71-1.37Hz)
Linear Range (Amperometry)	80p-0.5µA (210.5-787000Hz)
Input Referred Noise	13.8µV
Maximum Power Dissipation	16.71µW
Area	0.025mm^2
Linear range for improved sensor	
Linear Range (potentiometry)	0-1V (1.06-10.59Hz)

Improved sensor has less process variation for potentiometry.
Improved sensor has the function of states-transition.

working principle, detailed design consideration and simulation results are described in this chapter for both the potentiometry and the amperometry. This chapter also includes the layout, post-layout simulation and Monte-Carlo analysis of the proposed sensor.

Chapter 4 focuses on the improved version of the sensor. This chapter starts with some drawbacks of the initial design and then presents the corresponding solutions to improve the circuits. The improvement mainly includes expanding the linearity of the potentiometry for low input voltage, reducing the process variation of the potentiometry and adding the functionality of states-transition for the whole system.

Chapter 5 concludes the whole project, summaries what has been achieved and highlights the strengths of the system. Limitation of the project and further work are also discussed in this chapter.

Chapter 2

Project background

2.1 Biosensor

THE global biosensor market size was valued at USD 19.6 billion in 2019 and is anticipated to reach USD 36.0 billion by 2027 [12].

A biosensor, according to S.P.J. Higson, is a chemical sensing device in which a biologically derived recognition entity is coupled to a transducer, to allow the quantitative development of some complex biochemical parameters [13, 14]. Commonly, a biosensor could sense a biological element in biofluids and converts the response to an electrical signal [15]. The basic function of a biosensor could be represented in Figure 2.1 [16]. As shown in the figure, a biosensor could detect bioelements in analytes and convert the quantitative of the bioelements to electrical signals by a transducer (generally, electrodes and circuits). Some common analytes, bioelements, and electrical signals are also listed in the Figure 2.1.

Biosensors could be classified differently by different methods. In this report, biosensors are been classified based on the types of transduction [15, 17]. The classification of biosensors could be demonstrated as Figure 2.2

The underlying principle of an electrochemical biosensor is that when some chemical reactions happen, ions or electrons could be pordueced or consumed, which could cahnge the electrical properties of the solutions [16]. These changed electrical properties then
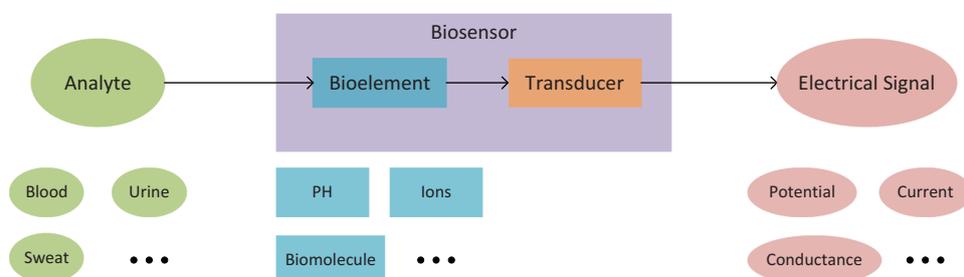
Figure 2.1: The working principle of a biosensor.
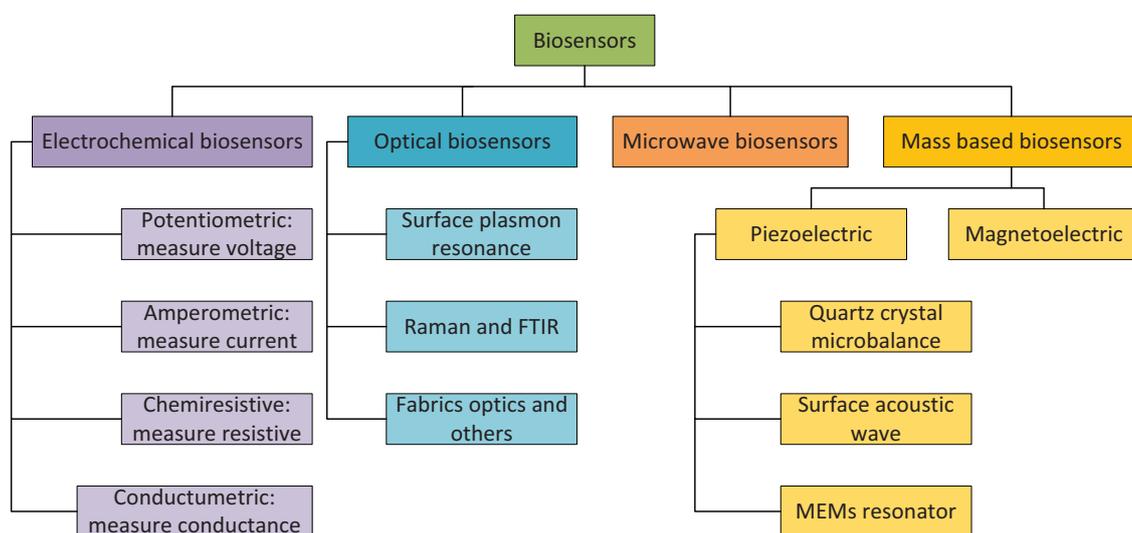
Figure 2.2: Classification of biosensors.

can be measured as parameters by electrochemical biosensors. Thus, the classification of electrochemical biosensors can be based on these changed properties and parameters, e.g. potentiometric, amperometric, chemiresistive, and conductimetric [16].

As for optical biosensors, the signal that is sensed is light [16]. The optical properties of the light could be changed due to the interaction between the analyte and the sensor. These properties include absorbance, reflectance, luminescence, fluorescence, refractive index, optothermal effect, and light scattering [15, 18–21].

In terms of microwave biosensors, the changed electromagnetic properties of the receptor in the sensor could be sensed, and the electromagnetic waves are often in the microwave range [15, 22]. Finally, mass-based biosensors could transform the mass change to the property (commonly, frequency) of the supporting material [15].

2.2   Potentiometry and amperometry – State of art

2.2.1   Potentiometry

In a traditional potentiometric biosensor, the potential difference between two electrodes is measured directly without involving current flowing [23]. Although there is a new method of potentiometry where a controlled DC current is applied to the analyte and then measure the resulting potential [23, 24], this report focuses on the former.

Therefore the potentiometry here is a simple voltage readout circuit. One possible solution is by using the voltage-controlled oscillator (VCO), in which the frequency of the output oscillation is related to the input voltage. However, typical VCO may not fulfil the requirement of linearity and sensitivity [25] for the potentiometry.

Another solution is converting the voltage to current linearly first, and then depending on the current readout circuit to measure the generating current. This topology is presented in Figure 2.3.

Here, specification of previous ressearch for potentiometry is listed in Table 2.1.

(a) Conventional V-to-I configuration.   (b) New V-to-I configuration [1].
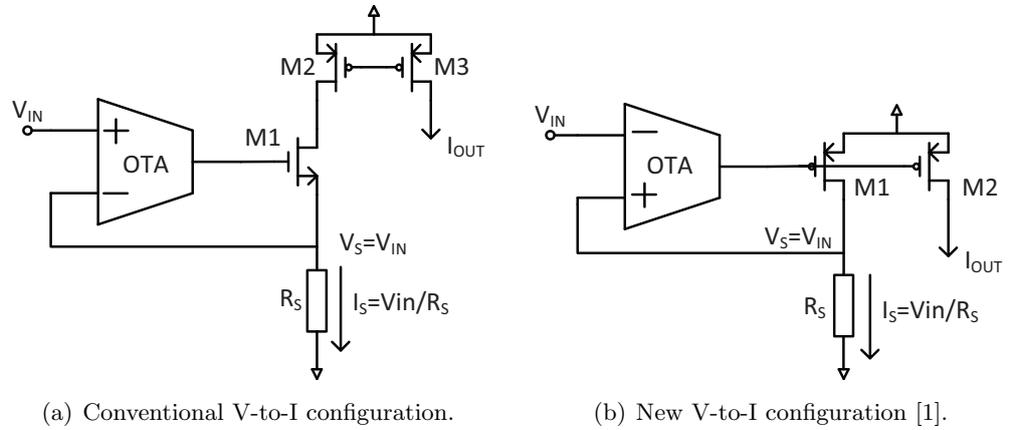
Figure 2.3: V-to-I configurations [1].

Table 2.1: State-of-art potentiometries in the literature.

Author&Year	Technology&Supply	Input Range	Sensitivity/V	Power
Wang, C. [26] 2006	0.25µm 2.5V	0-0.9V	520kHz	NA
Wang, C. [25] 2007	0.25µm 2.5V	0-0.9V	58MHz	0.22mW
Calvo, B. [27] 2009	0.35µm 3V	1.0-2.0V	1MHz	1.03mW
Azcona, C. [28] 2010	0.18µm 1.8V	0-1.6V	312.5/625 937.5kHz	400µW
Azcona, C. [29] 2011	0.18µm 1.2V	0-1.0V	490kHz	60µW
Calvo, B. [1] 2010	0.35µm 3V	0.1-2.7V	1MHz	800µW
Valero, M. R. [30] 2011	0.18µm 1.8V	0-1.2V diff. 1.2±0.6V	861kHz	0.375mW
Azcona, C. [31] 2012	0.18µm 1.2V	0-1.2V diff. 0.6±0.6V	750kHz	65µW
Koay, K. C. [32] 2018	0.18µm 1.5V	±0.024V	1.6MHz	0.1mW

2.2.2 Amperometry

In electrochemical literature, a sensor that applies DC voltage and measures the responding current is referred to as an amperometric sensor. Here, only the readout part of traditional amperometric sensors with DC current is studied.

Resistive and capacitive transimpedance amplifier readout circuit

A simple method of measuring the DC current is by converting the current to voltage and then measure the voltage. This could be done by adding a resistor or capacitor in the feedback network of a transimpedance amplifier (TIA), as illustrated in Figure 2.4 [23].

(a) Resistive transimpedance amplifier readout circuit.   (b) Capacitive transimpedance amplifier readout circuit.
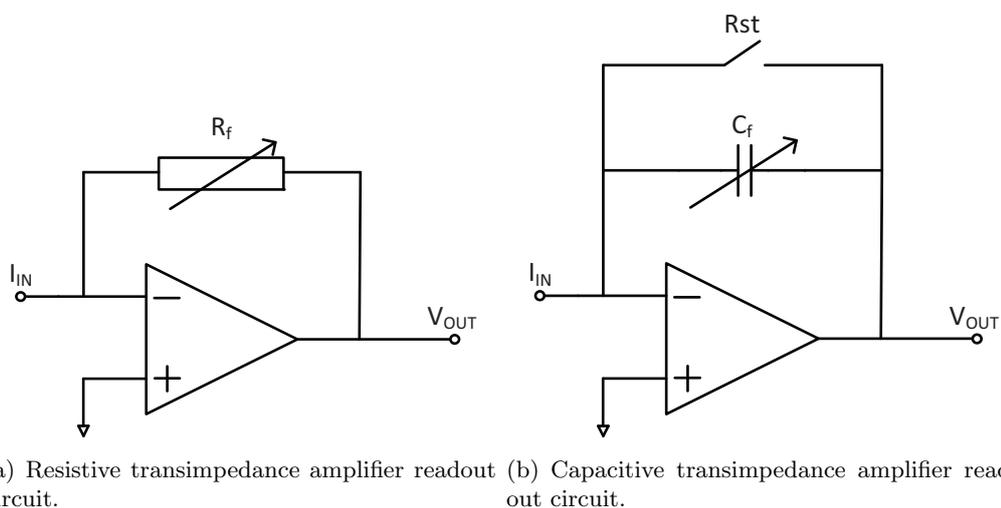
Figure 2.4: Resistive and capacitive transimpedance amplifier readout circuit.

The input current of resistive TIA readout circuit and capacitive TIA readout circuit can be calculated by equation (2.1) and equation (2.2), respectively.

$$I_{IN} = -\frac{V_{OUT}}{R_f} \tag{2.1}$$

$$V_{OUT} = \frac{1}{C_f} \int_0^T I_{IN} \, \mathrm{d}t \tag{2.2}$$

The capacitive feedback is preferred because a resistor could introduce more thermal noise than a capacitor does [23]. However, the input current resolution of capacitive

readout circuit is limited with the noise introduced by the switch in the feedback network [23]. Thus, correlated doubling sampling technique has been used to reduce the noise mentioned above and 1/f noise [33].

Current conveyor readout circuit

Current conveyor readout circuit could be used to read out the input current without introducing too much noise and consuming much power [23]. A simple and typical structure of current conveyor readout circuit is presnted in Figure 2.5 and the input current can be calculated by equation 2.3 [23].
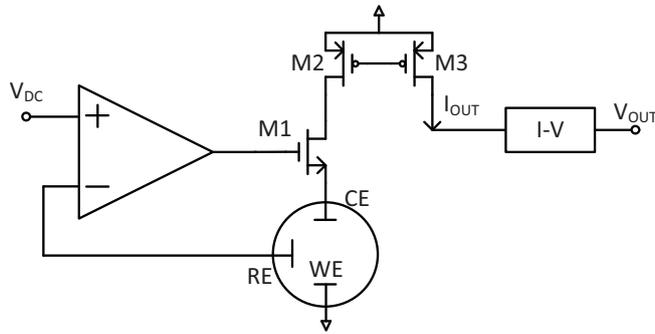
Figure 2.5: Current conveyor readout circuit [2].

$$\frac{I_{IN}}{I_{OUT}} = \frac{(W/L)_2}{(W/L)_3} \tag{2.3}$$

Current-to-frequency readout circuit

Many digitization circuits have been integrated with amperometric sensors [2,34,35]. Here, a commonly used topology called incremental first-order $\Sigma\Delta$ ADC structure is introduced. The benefits of this topology include high sensitivity, small area, and low power consumption [23]. The basic structure is illustrated in Figure 2.6.

Here, specification of previous study for amperometries is listed in Table 2.2.
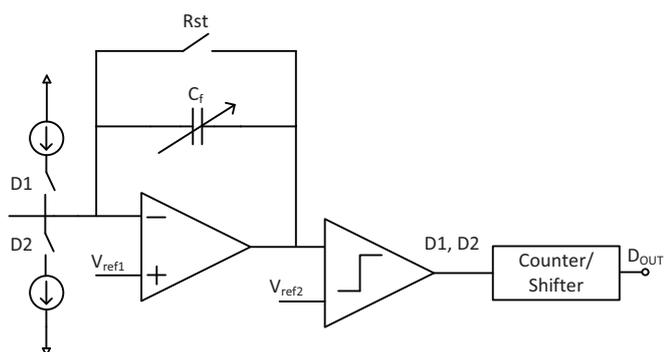
Figure 2.6: **Incremental first-order $\Sigma\Delta$ ADC structure for amperometric sensing.**

Table 2.2: State-of-art amperometries in the liturature.

Author&Year	Technology&Supply	Input Range	Input Noise	Power
Voulgari, E. [36] 2017	0.35μm CMOS 3V	0.003-3000nA	NA	NA
Baumann, S. [37] 2019	0.18μm CMOS 3.3V	0.001-1000nA	NA	NA
Voulgari, E. [38] 2019	0.35μm 3V	0.1-1000nA	NA	0.075mW

Chapter 3

Initial Design of Potentiometry and Amperometry

3.1 Overall Structure

THE overall structure of the dual potentiometry and amperometry is illustrated as Figure 3.1.
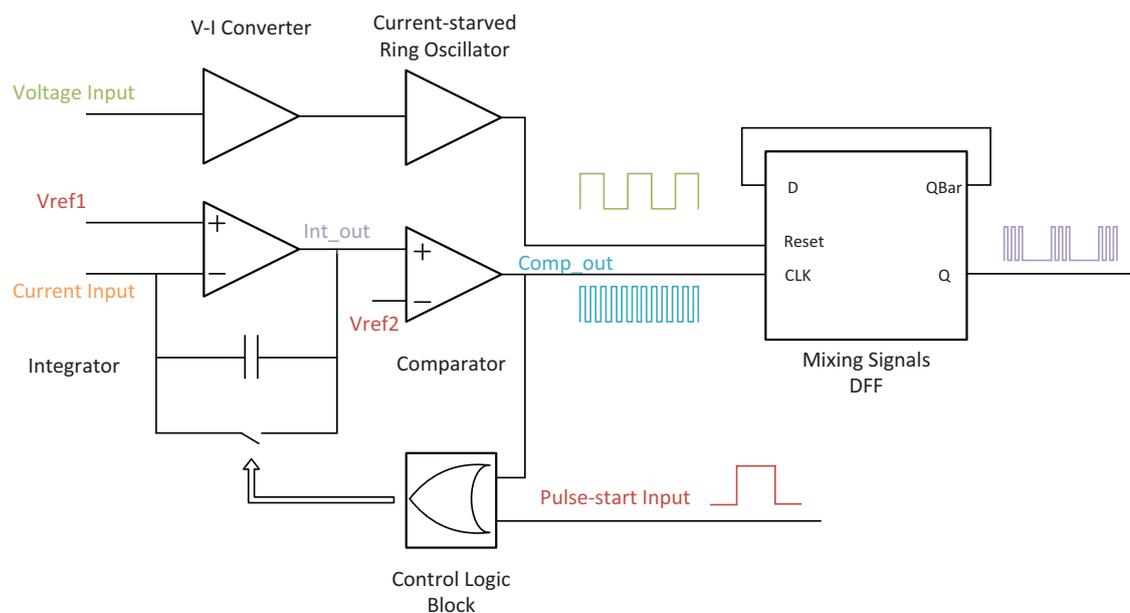
Figure 3.1: **The overall structure of the proposed sensor.**

The proposed potentiometry is basically a voltage-controlled oscillator, which could generate a square wave whose frequency is related to or controlled by the input voltage. In the design, the voltage input is first converted to current by a linear voltage-to-current converter as shown in Figure 3.1. The current then is sent to the **current-starved ring oscillator**, in which digital output is generated. The frequency of the output is correlated linearly with the current, hence linear to the input voltage.

Similarly, the function of the amperometry can be regarded as a current-controlled oscillator but is achieved by another approach – an adapted incremental first-order $\Sigma\Delta$ ADC. The oscillation is achieved by charging and resetting a known capacitor. The amperometry mainly consists of two parts: **an integrator** and **a comparator**. Input current charges the capacitor to change the potential of the node **Int_out**, the output signal of the comparator is generated by comparing **Int_out** with reference voltage **Vref2**. Meanwhile, the signal **Comp_out** is sent to the control logic block in the feedback network of the amperometry to make sure the potential of the node **Int_out** is within a specific range – between **Vref1** and **Vref2**.

The output of the potentiometry and the output of the amperometry then is mixed by a simple D-type flip flop (DFF). DFF could generate a waveform as shown in Figure 3.1.

3.2   Potentiometry

The proposed potentiometry is presented in Figure 3.2. As demonstrated in the figure, potentiometry includes two blocks: **V-I conversion** block and **current-starved ring oscillator** block. V-I conversion takes the voltage between the Ion-selective electrode (ISE) and reference electrode (RE) as the input – **In+**, converts the voltage to current linearly. The current-starved ring oscillator then takes the current as the input and generates the square waveform whose frequency is linearly dependent on the current.
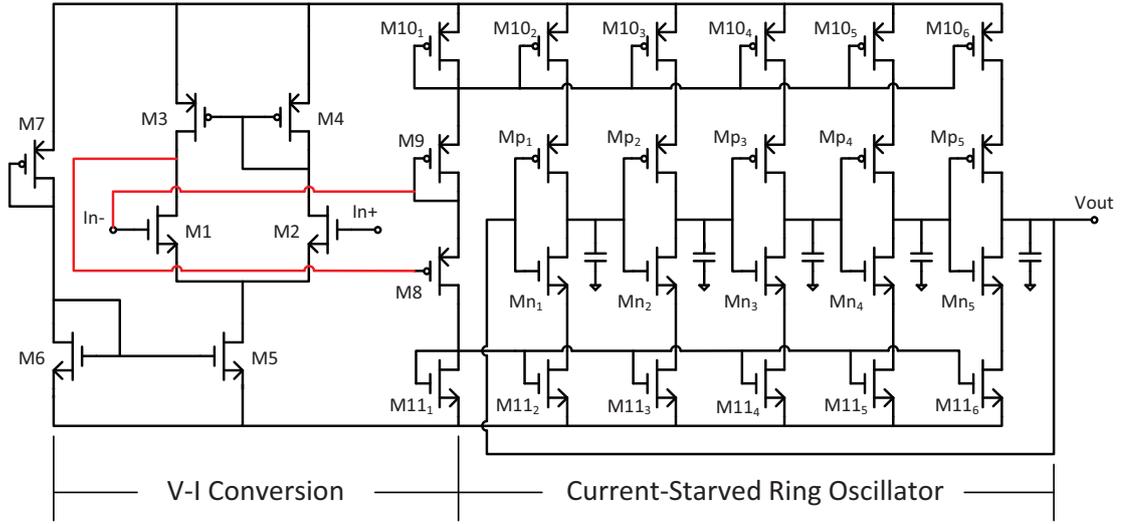
Figure 3.2: Schematic view of proposed potentiometry.

3.2.1 Voltage to Current Converter

The left part of Figure 3.3 presents the V-I conversion block of the potentiometry. The V-I converter takes the operational transconductance amplifier (OTA)/source follower negative feedback configuration [39]. The OTA is simply a differential pair as shown in the Figure 3.2. For low-power consideration, all the transistors in the OTA operate in the subthreshold/weak-inversion region. PMOS **M8** works as the source follower and the output of the follower would be sent to the negative input of the OTA to achieve negative feedback of the system. The potential of the node **X** then would force to be at the same potential with the positive input of the OTA, which is **Vin**.

PMOS **M9** and **M10$_1$** take the diode-connected construction and work as resistors. The resistance of diode-connected MOS in the small-signal model is $1/g_m$. The derivation of the resistance is presented in Figure 3.4 and equation (3.1). In order to lower the frequency of the output waveform and lower the power dissipation of the potentiometry, the width/length ratios of the two MOSFETs are choosing to be very small to achieve large resistance as explained by equation (3.2). Meanwhile, PMOS **M10$_1$** and NMOS **M11$_1$** work as a current source and a current sink respectively to mirror the current into each stage of the ring oscillator. It should be noticed that the width/length ratio of **M11$_1$** is
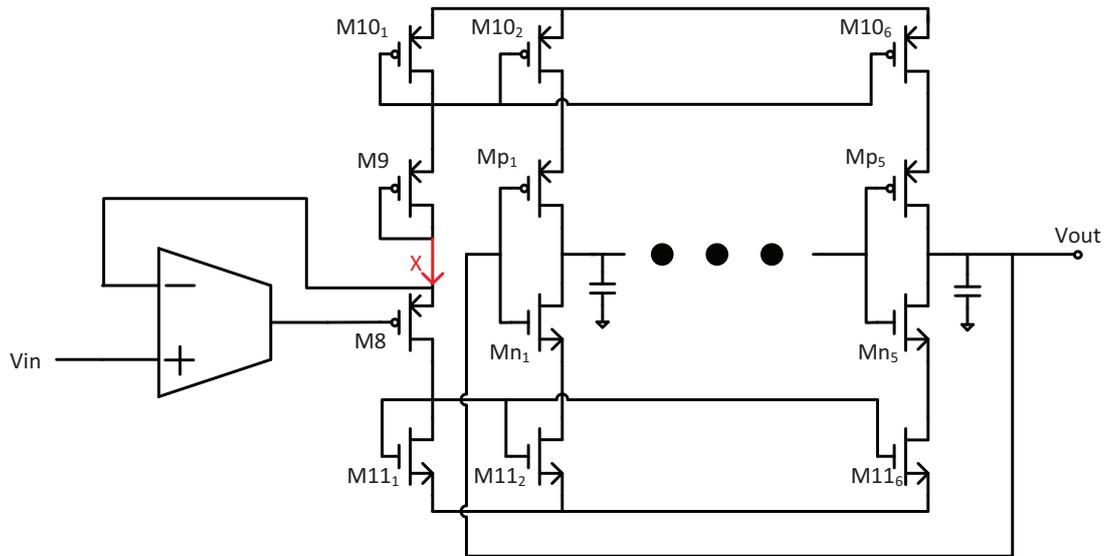
Figure 3.3: Illustration view of potentiometry.

much larger than **M11$_x$** at each stage of the ring oscillator, which serves to further reduce the current at each stage.
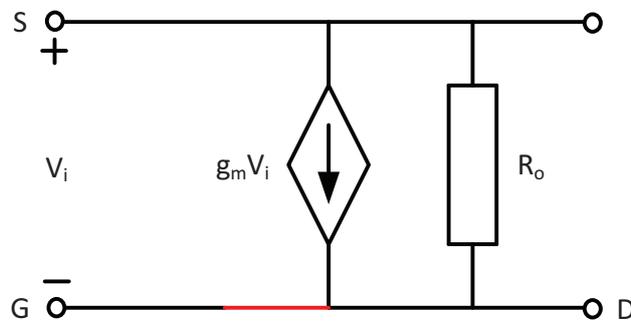
Figure 3.4: Equivalent small signal model of dioded connected PMOS.

$$
\begin{aligned}
R_{eq} &= R_o || \frac{V_i}{g_m V_i} \\
&= R_o || \frac{1}{g_m} \\
&\approx \frac{1}{gm}
\end{aligned}
\tag{3.1}
$$

$$I_d = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{sg} - |V_{THp}|)^2$$

$$g_m = \frac{\partial I_d}{\partial V_{sg}} = \mu_p C_{ox}\frac{W}{L}(V_{sg} - |V_{THp}|) \tag{3.2}$$

$$\frac{1}{g_m} = \frac{1}{\mu_p C_{ox}\frac{W}{L}(V_{sg} - |V_{THp}|)} \propto \frac{1}{\frac{W}{L}}$$

The current that flows through the node **X** then is calculated by equation (3.3).

$$I_x = \frac{V_{DD} - V_{in}}{R_{eq}}, \text{where } R_{eq} = \frac{1}{g_m(m10_1)} + \frac{1}{g_m(m9)} \tag{3.3}$$

Obviously, the potential of node **X** cannot be too low or too high, so that **M8**, **M11$_1$** or **M9**, **M10$_1$** drop into the triode region, and thus decrease the linearity of the V-I converter.

3.2.2   Current-Starved Ring Oscillator

The **current-starved ring oscillator**, as presented in the Figure 3.2, senses the current as the input and generates the square wave whose frequency is proportional to the value of the input current. The working principle is relatively simple, PMOS **M10$_1$** and NMOS **M11$_1$** mirror the current that flows through the node **X** into each stage of the oscillator, while PMOS **Mp$_x$** and NMOS **Mn$_x$** operate as inverters. The five-stage inverter connects one-by-one in a loop and the whole becomes a ring oscillator.

However, there are some details that need to be mentioned in the design. For a traditional current starved ring oscillator, as presented in Figure 3.5(a), the frequency mainly depends on the input current and the internal capacitance of the inverter. While in this design, the frequency of the output square wave needs to be very low (see Section 3.3.2), which requires the input current to be very small and the capacitor to be very large. The extreme small current is achieved by using a very large resistor (long transistor with gate and drain connected) and current mirror to scale down the current. The large capacitor is achieved by using large transistors at each stage and adding an external capacitor at the

output of each stage as shown in Figure 3.5(b). The scaling factor of the current mirror is extremely large - $\frac{60/10}{0.22/20}$, which could not be achieved in practice. However, the purpose of the large scaling-down factor is to make sure the frequency of the output signal is low enough, and the real value of scaling factor in the circuit is not crucial.
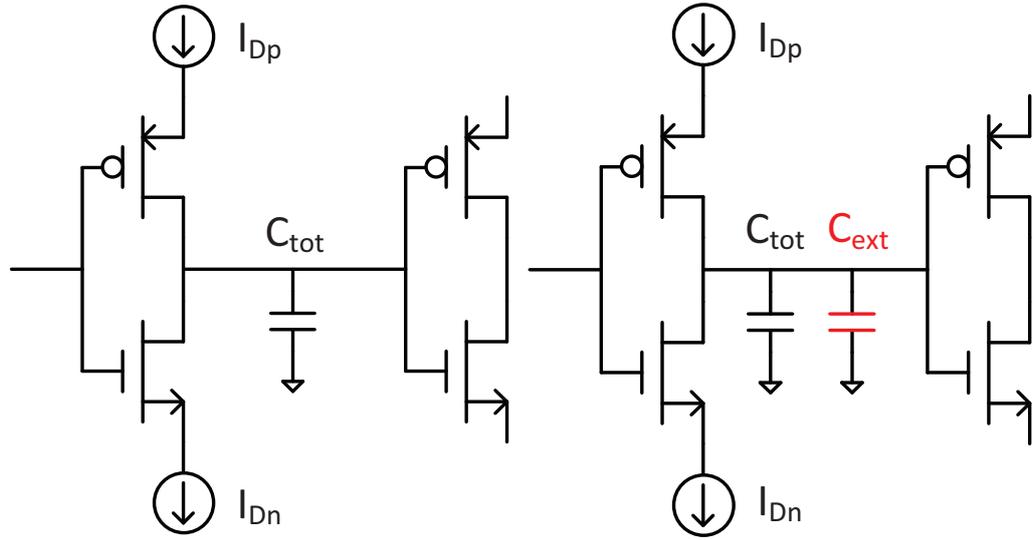
(a) A single stage inverter with internal capacitance. (b) A single stage inverter with external capacitance.

Figure 3.5: Illustration of capacitance in each stage of ring oscillator.

The internal capacitor can be calculated using equation 3.4), while the overall capacitance at the output of each stage is given by equation (3.5).

$$
\begin{aligned}
C_{tot} &= C_{out} + C_{in} \\
&= C'_{ox}(W_p L_p + W_n L_n) + \frac{3}{2}C'_{ox}(W_p L_p + W_n L_n) \\
&= \frac{5}{2}C'_{ox}(W_p L_p + W_n L_n)
\end{aligned}
\tag{3.4}
$$

$$
C_{all} = C_{tot} + C_{ext} = \frac{5}{2}C'_{ox}(W_p L_p + W_n L_n) + C_{ext}
\tag{3.5}
$$

The time it takes to charge the capacitor to the switching point with current I_{Dp} can be calculated using equation (3.6), and the time to discharge the capacitor from the supply voltage to the switching point with current I_{Dn} is given by equation (3.7).

$$t_1 = C_{all} \cdot \frac{V_{sp}}{I_{Dp}} \tag{3.6}$$

$$t_2 = C_{all} \cdot \frac{V_{DD} - V_{sp}}{I_{Dn}} \tag{3.7}$$

For simplicity, assuming I_{Dp} is equal to I_{Dn} and the switching point V_{sp} is approximately VDD/3. Thus, the period of the single-stage inverter is given by $T_{inv} = t_1 + t_2 = C_{all} \cdot \frac{V_{DD}}{I_D}$. The frequency of the 5-stage ring oscillator then is $T = \frac{T_{inv}}{5} = C_{all} \cdot \frac{V_{DD}}{5I_D}$.

The width of the transistors at the last stage of the oscillator is relatively larger than other stages to improve the driving capacity of the oscillator.

3.2.3   Simulation Results of Potentiometry

The potentiometry has been designed in **TSMC180BCD** technology with supply voltage of 1.4V. In the Figure 3.2, the sizes of the differential pair (**M1**, **M2**) are set to 60µm/1.2µm, and the current mirror load (**M3**, **M4**) are set to 30µm/1.2µm. The biasing current is introduced to the differential pair by a current mirror (**M5**, **M6**) with a gain of 2. The source current is generated by putting a large resistor between VDD and the drain of transistor **M6**. The large resistor is implemented by a diode-connected transistor **M7**. The sizes of **M5**, **M6**, **M7** are 20µm/0.5µm, 10µm/0.5µm and 500nm/5µm, respectively. The biasing current is designed to be 2µA approximately to reduce power. The sizes of the rest transistors in the potentiometry are listed in Table 3.1.

Table 3.1: Size of transistors in the potentiometry.

MOSFETs	W/L
M10$_1$, M10$_2$, M10$_3$, M10$_4$, M10$_5$ M11$_2$, M11$_3$, M11$_4$, M11$_5$	220nm/20µm
M11$_1$	60µm/1µm
M8	220nm/10uµm
M9	5uµm/5µm
Mp$_{1-4}$, Mn$_{1-4}$	2µm/20µm
M10$_6$, M11$_6$, Mp$_5$, Mn$_5$	10µm/180nm

The linearity and the power consumption of the potentiometry are presented in Figure 3.6. The linear input range for potentiometry is **0.3-1V**, the sensitivity is about **12.3Hz per decade**. The power dissipation is quite low and is lower than **4.5μW**.
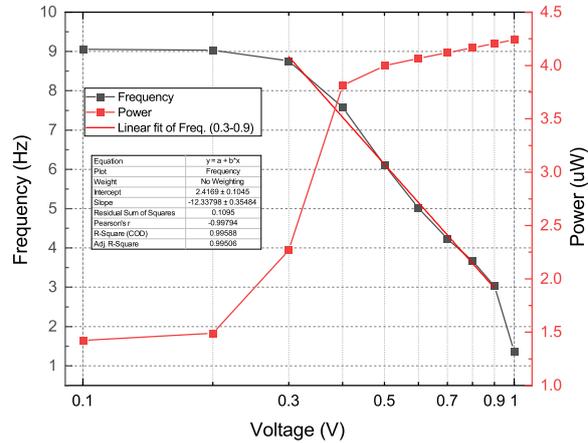
Figure 3.6: Linearity and power consumption for potentiometry.

3.3   Amperometry and Singal-Mixing Block

3.3.1   Phase Analysis in Amperometry

The topology used in the amperometry is the adapted incremental first-order $\Sigma\Delta$ ADC mentioned above. There are two working phases in the amperometry: the **resetting phase** and the **charging phase**. The start of the amperometry is triggered by an external signal – power-on reset, which is essentially a single pulse and marked as **pulse-start input** in the Figure 3.1. This signal could force the amperometry into the resetting phase and short the capacitor. Consequently, the integrator becomes a **unity-gain buffer** as illustrated in Figure 3.7, the left and the right plate of the capacitor would be of the same potential as the positive input – **Vref1**. Meanwhile, the **Int_out** is higher than **Vref2**, the output of the comparator – **Comp_out** would give the low level of the square wave, which contribute nothing to the **or** gate and could not change the phase of the amperometry.

When the power-on reset signal comes low, the **or** gate would give the zero potential
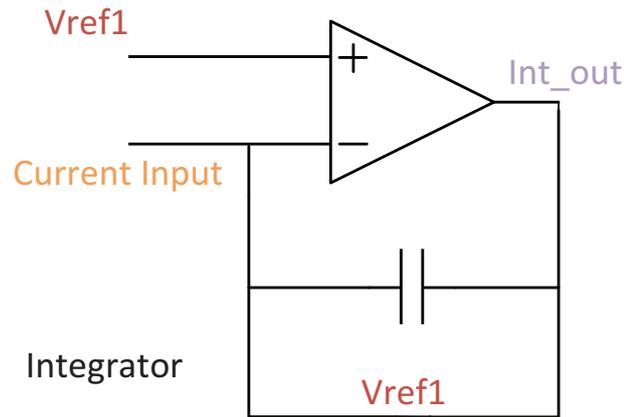
Figure 3.7: In resetting phase, the integrator becomes a unity-gain buffer.

and drive the amperometry to the charging phase as shown in Figure 3.8. The integrator would integrate the input current, which results in a potential difference between the two plates of the capacitor. Since the potential of the left plate of the capacitor is fixed, the potential of the right plate, **Int_out**, would dropdown gradually. When **Int_out** reaches or drops below **Vref2**, the output of the comparator - **Comp_out** would flip over and give a high potential which would trigger the **or** gate and close the switch. The amperometry would than return to the resetting phase, and wait for the **Comp_out** to be high again.
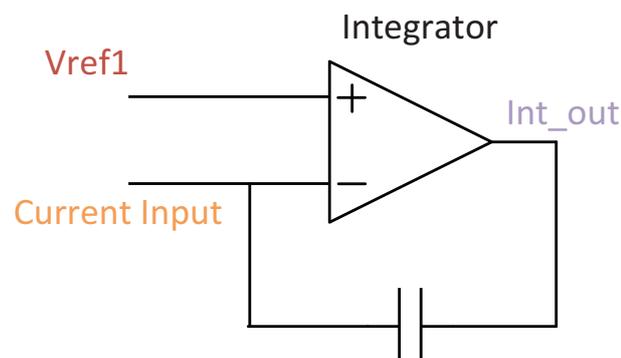
Figure 3.8: Integrator in the charging phase.

The variation of **Int_out** and **Comp_out** is demonstrated in Figure 3.9, where $\mathbf{t_1}$ represents the period of the charging phase, while $\mathbf{t_2}$ represents the period of the resetting phase. $\mathbf{t_1}$ can be calcultated by equation (3.8). When duration of resetting phase is much shorter than charging phase, $\mathbf{t_2}$ can be ignored and $\mathbf{t_1}$ is dominant in the period of the

amperometry. Thus the frequency of the amperometry is $f_{amp} = \frac{1}{t_1} = \frac{I_{In}}{C \cdot (Vref1 - Vref2)}$, which is proportional to the input current.
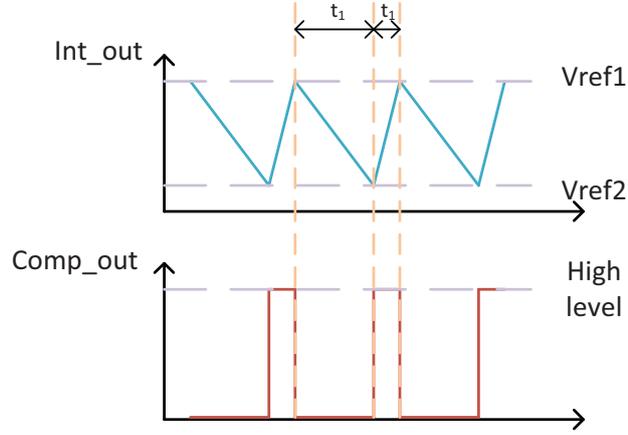
Figure 3.9: **The waveform of Int_out and Comp_out.**

$$t_1 = \frac{C \cdot (Vref1 - Vref2)}{I_{In}} \tag{3.8}$$

It is can be foreseen that when the input current is large, $\mathbf{t_2}$ is comparable with $\mathbf{t_1}$ and $\mathbf{t_2}$ cannot be ignored, the linearity of the amperometry would decay.

3.3.2 Signal-Mixing Block

The signal-mixing block is very simple and consists of a DFF with an asynchronous **reset** port. As presented in Figure 3.1, the output of potentiometry is sent to the **reset** port of the DFF and the output of amperometry goes to the **clock** port of DFF. The output port **QBar** is connected to the input port **D** to achieve flipping over when **reset** is inactive and DFF encounters the rising edge of the **clock**. The system output is taken from the output port **Q**. The relation of the output of potentiometry, amperometry, and the whole system is presented in Figure 3.10.

As shown in the Figure 3.10, the frequency of the potentiometry and the amperometry should be apart from each other to avoid the aliasing problem when reading out from the system output. However, there exits an error when taking the output from port
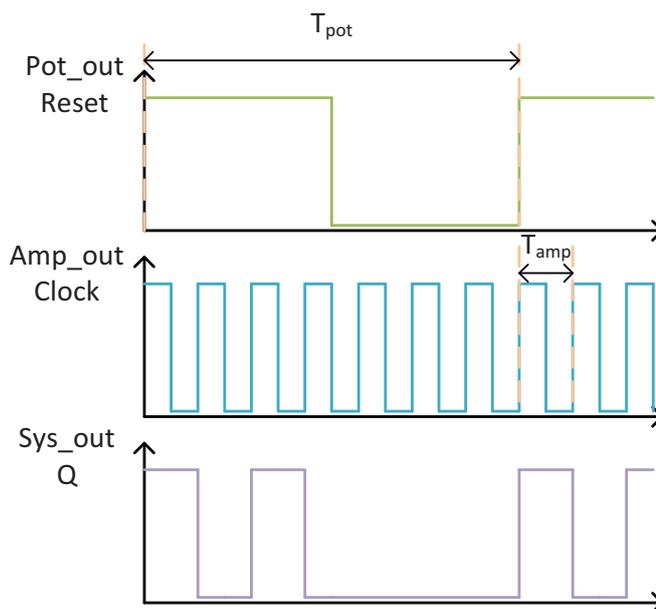
Figure 3.10: **The output waveforms of potentiometry, amperometry and the whole system.**

Q. When the rising edge of **Amp_out** occurs before the rising edge ot **Pot_out**, **Sys_out** could not record the first period of **Amp_out**, and cause errors of frequency for potentiometry. The maximum error is the miss of a whoel period of **Amp_out**, and can be calculated by equation (3.9).

$$e_{max} = \frac{T_{amp}}{T_{pot}} \tag{3.9}$$

Thus, in order to control the error to be less than 10%, the frequency of the amperometry **Amp_out** should be at least ten times the frequency of the potentiometry **Pot_out**. This is achieved by splitting the frequency ranges of the potentiometry and the amperometry apart from each other, and blocking the output of amperometry when the frequency is too low.

As a matter of fact, the high level of **Comp_out** cannot reach the supply voltage 1.4V and **Comp_out** is proportional to the input current. The high level of **Comp_out** is approximately 650 mV when the input current is 100 pA, while **Comp_out** could reach 680 mV when the input current is 10 nA. This is due to the fact that larger input current could ramp **Int_out** higher, which, consequently, slower the resetting phase and

the output of the comparator **Comp_out** could have more time to slew up and reaches higher potential.

On the other hand, the **or** gate takes Nand construction as shown in Figure 3.11 [40]. Thus the switching point of the **or** gate is lower than a normal inverter, which is actually inside the DFF and takes the clock signal as the input and generates the opposite phase of the clock. Therefore, there is a point when **Comp_out** reaches the switching point of the **or** gate, but not high enough in terms of the switching point of the inverter in the DFF. In this scenario, DFF could not generate output properly. In this proposed amperometry, the switching point of the inverter in DFF is tuned at the point when the input current is 80 pA and the frequency of amperometry for 80pA input is approximately 400 Hz.
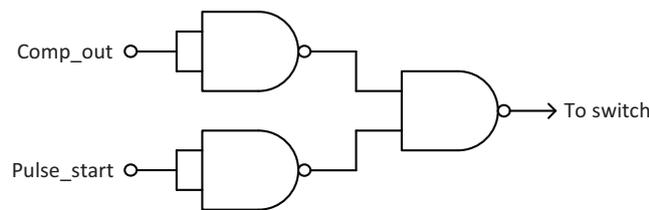
Figure 3.11: **The Nand construction of or gate.**

3.3.3   Simulation Results of Amperometry

The integrator and the comparator both takes the simple differential pair, which is the same as the one in the potentiometry. There is an inverter at the output of the comparator to improve the slew rate of **Comp_out** a little bit. The DFF takes master-slave edge-trigger construction with an asynchronous reset port [41]. The control logic is an **or** gate and takes the Nand construction. The integrated capacitor is **0.5pf**.

The simulation results of amperometry is shown in Figure 3.12. Both the x-axis - input current and the y-axis - frequecny are in logarithmic scale. The linear input range for amperometry is **80pA - 1μA** and the sensitvity is **0.94log(Hz)/log(A)**. The power dissipation is below **15μW**.
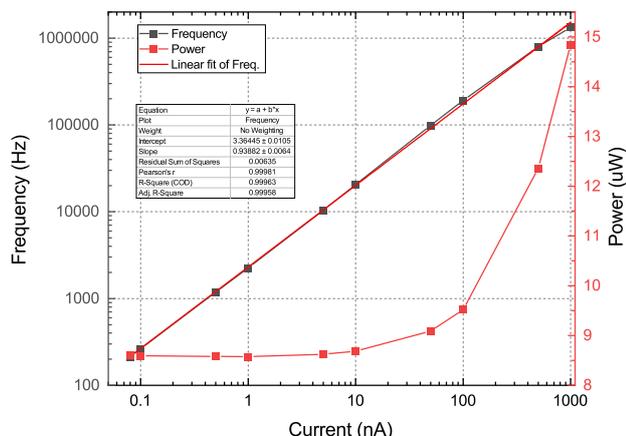
Figure 3.12: The linearity and power dissipation of amperometry.

3.4 Systematic Simulation

The potentiometry and the amperometry have been combine together as shown in Figure 3.1 and have been simulated in cadence. The systematic simulation results show consistance with the simulation of potentiometry or amperometry alone. Some of the results are presented in Figure 3.13. The specification does not change, which means the potentiometry and the amperometry do not interact with each other.
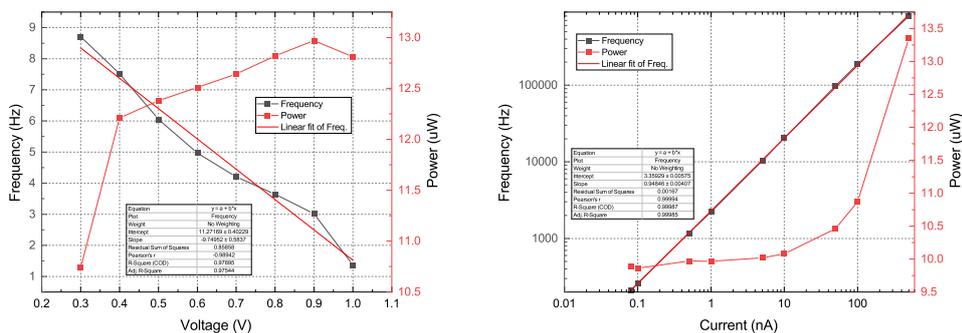
(a) Systematic simulation results for potentiometry (input current is fixed at 80pA).

(b) Systematic simulation results for amperometry (input voltage is fixed at 0V).

Figure 3.13: Systematic simulation of potentiometry and amperometry.

3.4.1 Layout and Post-Layout Simulation

The layout has been done for this sensor and is presented in Figure 3.14.
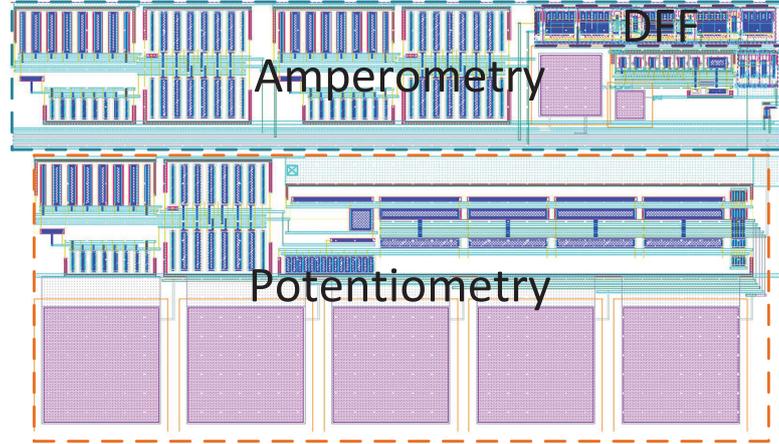
Figure 3.14: **The layout of the proposed sensor.**

The post-layout simulation has also been done with Calibre. The simulation results are shown in Figure 3.15. The linearity of potentiometry and amperometry are kept, while there is some shift of frequency versus inputs, especially for potentiometry. This is due to the parasitic capacitance between the output at each stage of ring-oscillator and the ground. This could be reduced if further improve the layout. It is also should be noticed that the minimum input current that could trigger the clock of DFF now is 60pA (in previous simulation, it is 80pA), which is fine for controlling the error below 10% sicne the frequency of amperometry is still much larger than that of the potentiometry.

3.4.2 Monte-Carlo Simulation

Monte-carlo analysis has been done for this project, and the results are shown in Figure 3.16. As it is presented in the figure, the process variation is much larger than mismatch variation for both potentiometry and amperometry. However, the process variation is acceptable for amperometry since the frequncy of amperometry is very high, and the percentage of standard deviation is $\frac{79.35}{517.5} = 0.15$, while the percentage of standard deviation for potentiometry in process simulation is $\frac{1.79}{6.49} = 0.276$. The large process variation
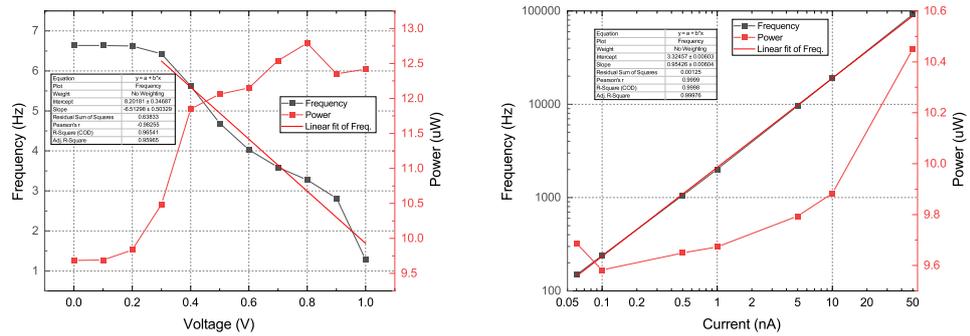
(a) Post-layout systematic simulation for poten-
tiometry (input current is fixed at 60pA).

(b) Post-layout systematic simulation for am-
perometry (input voltage is fixed at 0V).

Figure 3.15: Post-layout systematic simulation for potentiometry and Amperometry.

is reported by Zhang [42]. According to Zhang, the variation is due to the variation of
current, and a solution called subtraction-based voltage-controlled current source [42] has
been introduced to reduce the variation. However, in this report, another solution has
been used and will be introduced in Chapter 4.
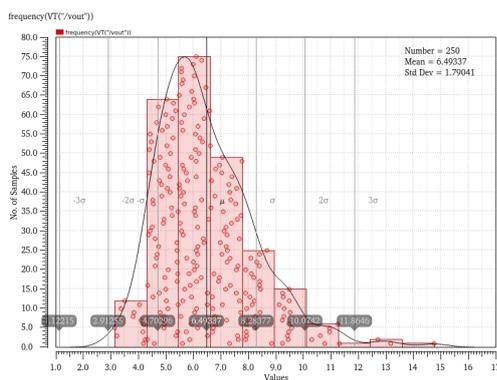
(a) Process variation for potentiometry.
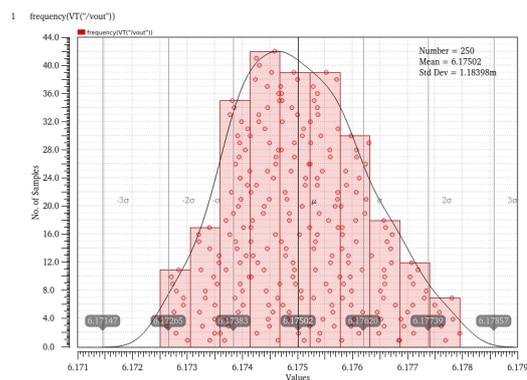
(b) Mismatch variation for potentiometry.
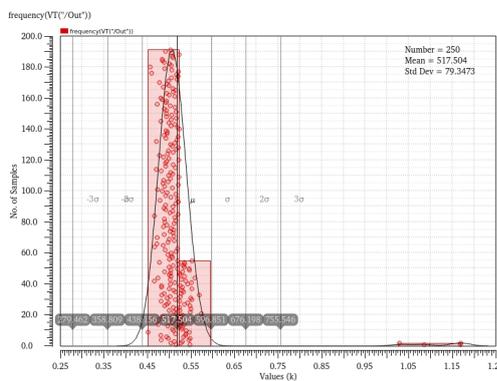
(c) Process variation for Amperometry.
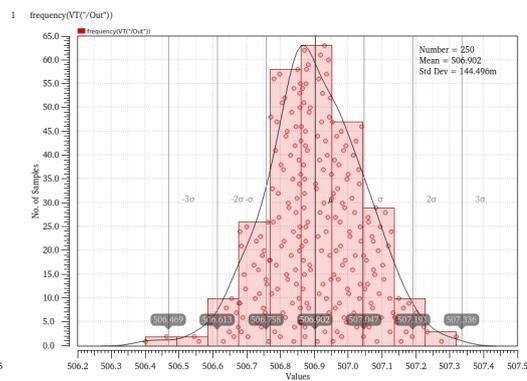
(d) Mismatch variation for Amperometry.

Figure 3.16: Monte-carlo simultation of proposed sensor.

Chapter 4

Improved Design of potentiometry and amperometry

4.1   Improved potentiometry

IN the initial design of the potentiometry, the linear input range is **0.3-1V**, which is not perfect for a biosensor. The minimum input is **0.3V**, which means the sensor could not distinguish the input if the voltage is below 0.3V. Another drawback of the potentiometry is the process variation. The percentage of standard deviation is **0.276**, which makes it hard to calibrate.

Thus, an improved potentiometry design is introduced and the schematic of the design is presented in Figure 4.1. Previously, in Figure 3.3, when the input voltage is very low and the node **X** would be at the same potential of the low input, NMOS **M11$_{1-6}$** would be shut down and the linearity of potentiometry would be destroyed. Additionally, there is only one stage of current mirror to scale down the current but with an extremely large scaling factor in previous design. This structure would bring a huge variation in Monte-Carlo process simulation.

Here, in Figure 4.1, the OTA/source follower construction is kept, while the potential of node **X** would not affect the MOSFETs in the ring-oscillator, since node **X** is split from the oscillator. This could improve the linearity with low voltage inputs. Fur-
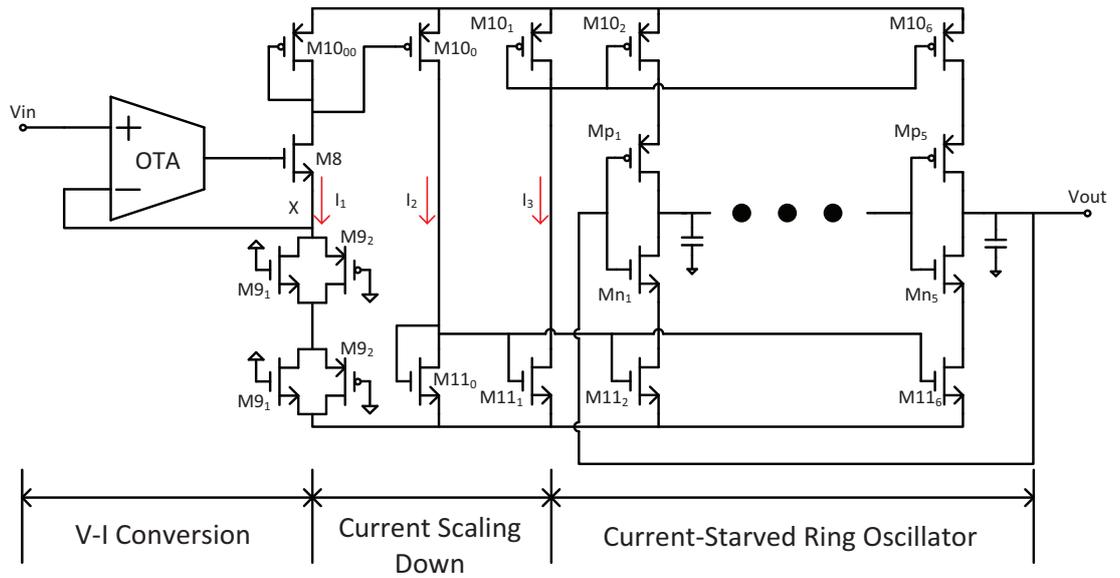
Figure 4.1: The schematic of the improved potentiometry.

thermore, the diode-connected transistor is changed with parallel-connected PMOS and NMOS to obtain relatively constant resistance even with the change of potential at node **X** [1].

In terms of the process variation, the improved design introduced one more stage to scale the current. The current I_1 is first scaled down to I_2 by current mirror $M10_{00}$ and $M10_0$, and then I_2 is scaled down by current mirror $M11_0$ and $M11_{1\text{-}6}$. This technique effectively reduces the process variation of the potentiometry.

The comparison of simulation results between the new topology and the previous design is presented in Figure 4.2, and the comparison of Monte-Carlo process simulation is given in Figure 4.3. As mentioned above, the linearity of the improved potentiometry is better than the initial design, especially when the input voltage is low. Additionally, the percentage of the standard deviation in Monte-Carlo process simulation now is **0.126**, which is much better than that of the previous design.
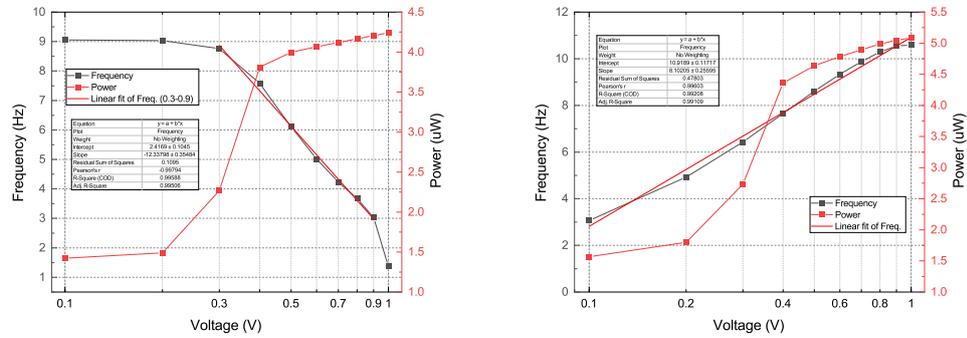
(a) Simulation results of previous design of potentiometry.

(b) Simulation results of improved design of potentiometry.

Figure 4.2: Comparison of simulation results for initial and improved potentiometries.
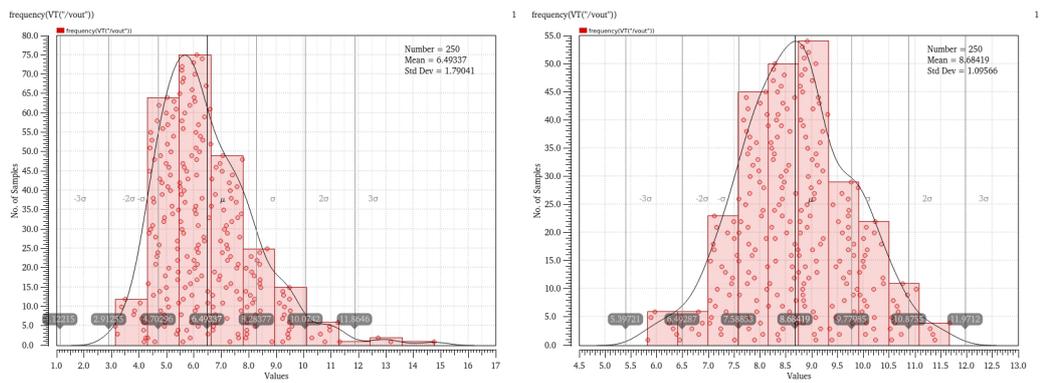
(a) Monte Carlo process simulation of previous design of potentiometry.

(b) Monte Carlo process simulation of improved design of potentiometry.

Figure 4.3: Comparison of Monte Carlo process simulation between initial design and improved design

4.2   Function of states transition

In the improved sensor, the function of the state-transition has been added. The function is achieved by adding two external control bits a_1 and a_2, and the sensor would work at different modes based on these control bits. When a_1 and a_2 are both 0, the sensor does not work and gives 0 output. When a_1 is 0 and a_2 is 1, the sensor works at amperometric mode, gives the output of the amperometry alone. When a_1 is 1 and a_2 is 0, the sensor works at potentiometric mode, and only gives the output of the potentiometry. Last, when a_1 and a_2 are both 1, the sensor works at dual amperometric and potentiometric mode and behaves just like the previous design.

In order to achieve this function, the previous DFF is replaced with a new DFF with an asynchronous set and an asynchronous reset ports, as shown in the Figure 4.4, both set and reset ports are low-active. In addition, some logic gates are added to control the sensor. The main task is to find the logic combination of **clk**, **set** and **reset** ports.
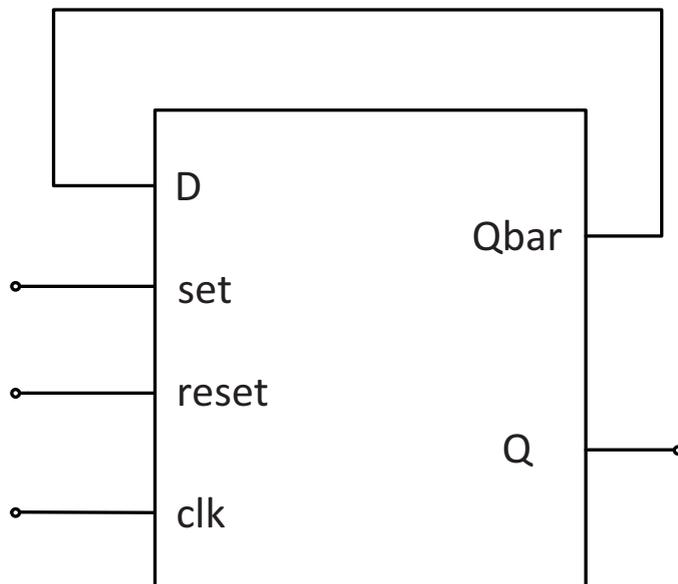
Figure 4.4: DFF with asynchronous reset and set ports.

4.2.1   Logic for Clk Port

Previously, **clk** is connected to the output of amperometry **Comp_out**, while in the new design, **clk** is determined by the combination of **Comp_out** and a_2. **Clk** follows the rules below:

- When a_2 is 0, **clk** should be fixed.

- When a_1 is 1, **clk** should follow **Comp_out**.

Thus, the logic expression for **clk** is $clk = \overline{a_2} + Comp\_out = \overline{a_2 \cdot \overline{Comp\_out}}$, and the logic gate is shown in Figure 4.5.
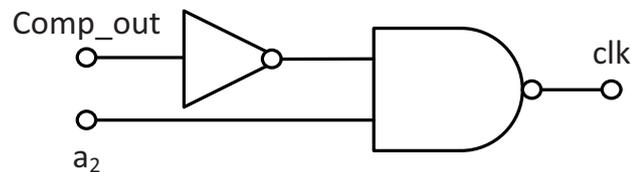
Figure 4.5: The logic gate for clk.

4.2.2   Logic for Reset Port

The **reset** port is determined by a_1 and **Pot_out**, and follows the rules:

- When a_1 is 0, the potentiometry should be shut off, and **reset** is 1.

- When a_1 is 1, **reset** should follow the **Pot_out** to make sure potentiometry works properly.

Thus, the logic expression for **reset** is $reset = \overline{a_1} + Pot\_out = \overline{a_1 \cdot \overline{Pot\_out}}$, and the logic gate is shown in Figure 4.6.

4.2.3   Logic for Set Port

The logic combination for **set** port is a little bit complicated, since it involves three signals: a_1, a_2 and **Pot_out**. The Karnaugh map is used to determine the logic expression of **set** and is shown in Figure 4.7.
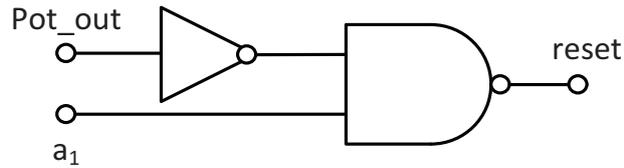
Figure 4.6: The logic gate for reset.

Figure 4.7: The Karnaugh map for set.

Thus the logic expression of **set** is $set = \overline{a_1} + a_2 + \overline{Pot\_out} = a_2 + \overline{a_1 Pot\_out}$, and the logic gate for this expression is shown in Figure 4.8.
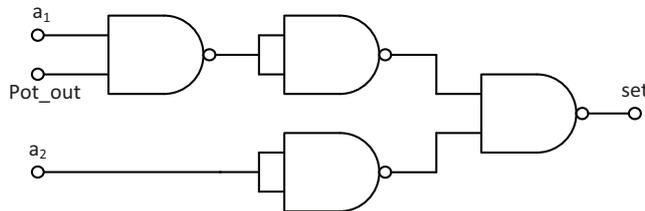
Figure 4.8: The logic gate for set.

4.3   Timing Diagram of Improved Sensor

The timing diagram of the improver sensor has been extracted from the simulation and is shown in Figure 4.9. As it can be seen, the functionality of the state-transistion could work pretty well in the improved sensor, the four different modes with their input control bits and output signals are marked in the figure.
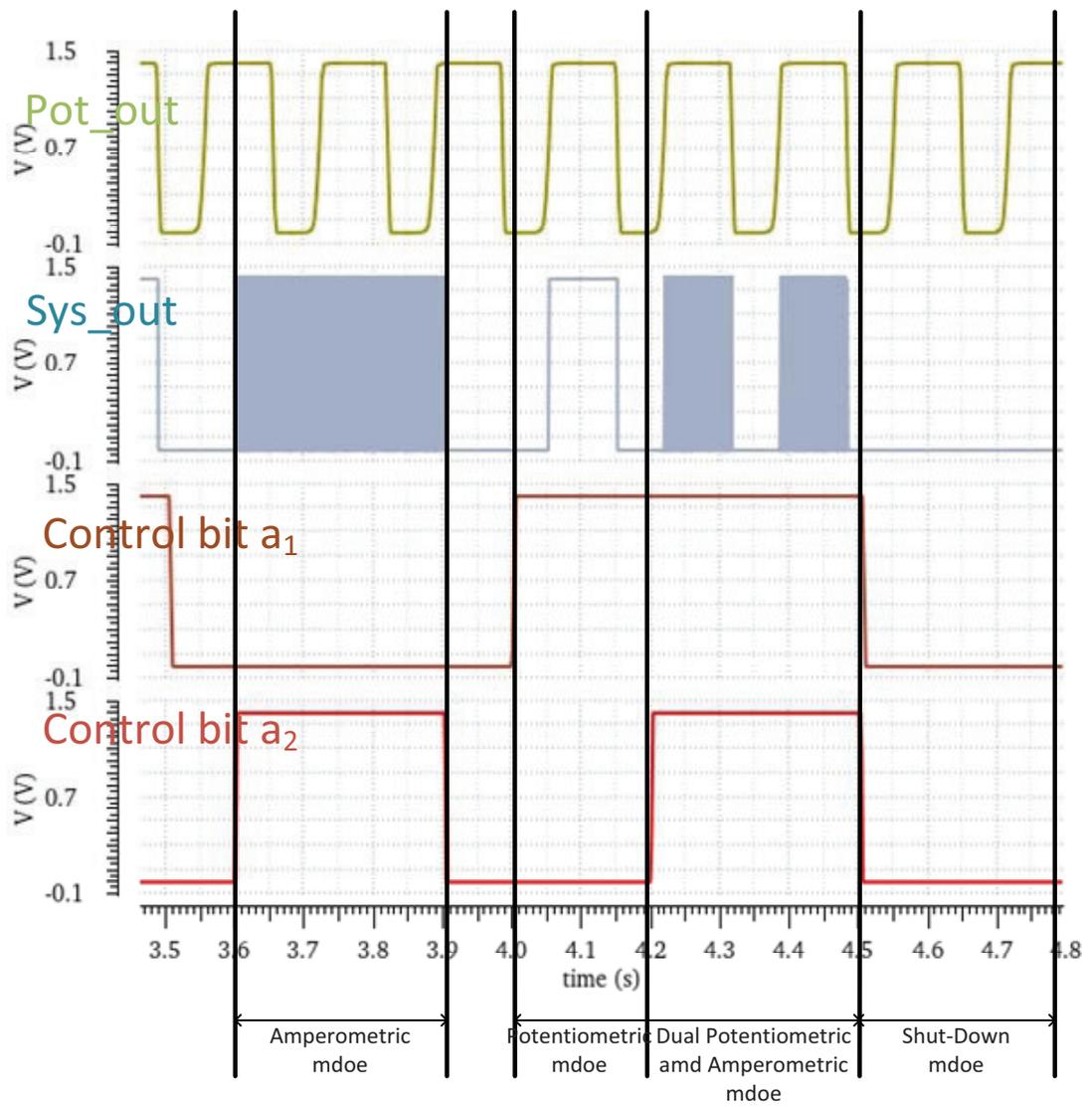
Figure 4.9: Timing diagram of improved sensor.

Chapter 5

Conclusion and Future Work

5.1   Conclusion

This project aims at designing a portable biosensor, which includes a potentiometry, an amperometry and a mixing-signal block. This sensor detects the voltage and current inputs from the electrodes and converts them to an asynchronous square wave as the output. The output consists of square waves with two frequencies, the slow one corresponds to the voltage input, while the other represents the current input. This single output is easy to read out, process and is suitable for wireless data transmission.

The design consideration and simulation results are presented in this report, this proposed sensor works well with the voltage input of 0.3-1V and current input of 80pA-1uA. The power dissipation of the sensor is quite low with the maximum power of 16.71uW. The layout of the sensor has been done and the post-layout simulation has been constructed in cadence. The post-layout simulation shows some shift of frequency for potentiometry. Additionally, Monte-Carlo analysis has been done and presents a large process variation of the potentiometry.

In order to expand the linear range of potentiometry at low input voltage and reduce the process variation, an improved version of potentiometry has been introduced. The improved potentiometry splits the current scaling-down process into two stages and effectively alleviate the constrain of the minimum voltage input and reduce the process

variation.

Furthermore, the function of states-transition has been added to the improved sensor. This function is achieved by adding two extra control bits. There are four states in the system: shut-off state, potentiometric state, amperometric state, and dual potentiometric and amperometric state, corresponding to the four states of the two control bits. The timing diagram of the simulation results shows the function of state-transition works well in the improved sensor.

5.2   Future Work

Due to the time limitation of the project, some work could not be constructed and is listed as follows:

- The taped-out chip cannot be tested within the time frame.

- The layout for the initially designed sensor should be improved since there is a shift of frequency for potentiometry.

- The layout and post-layout simulation of the improved sensor should be done.

- The function of state-transition could be designed to reduce power, since some part of the sensor does not have to work.

- More simulation should be constructed for the improved sensor.

- Other topologies should be compared with the proposed sensor.

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