Imperial College London

Department of Electrical and Electronic Engineering

E3-02 - AO13 Instrumentation Spring 2020

Coursework Design Brief

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Chapter 1

A Vector Impedance Meter

1.1 Description

We are all familiar with the resistance meter, which measures the value of a resistor by applying a current and measuring a voltage. This instrument. can measure resistances but it cannot measure devices which exhibit energy storage, such as capacitors and inductors.

Many sensors, diodes and other microelectronic devices show capacitive energy storage so that they behave like one of the following:

- A capacitor with a relatively small resistor in series
- A capacitor with a relatively big resistor in parallel

Other sensing devices, such as microphones and some inertial sensors behave like lossy inductors, namely inductors in series with a resistance.

Finally, many two terminal devices display a resonant behavior, namely some sort of combination of resistance, capacitance and inductance. This is typical of coils at higher frequencies and antennas.

In most of these measurements both the real and the imaginary part of the impedance change with frequency. To determine which "equivalent circuit" model is most suitable as a model for a particular device, the measurement needs to be performed at more than one frequency.

Specialised equipment which can measure complex voltages or complex impedances do exist; they are referred to by several different names, depending on their operation principle:

- Complex impedance meters
- Network Analysers
- Lock-in amplifiers
- Vector signal analysers

1.1.1 Impedance vs Admittance

In this assignment we are dealing with two-terminal devices. The concepts of impedance and admittance are interchangeable. To measure the complex impedance two tactics can be followed:

- 1. Apply a voltage and measure a current in amplitude and phase (admittance)
- 2. Apply a current and measure a voltage in amplitude and phase (impedance)

The choice of the mode of measurement is dictated by the sensitivity of the instrument used: Large in magnitude impedances are measured as impedances, while small in magnitude impedances are measured as admittances. As a rule, the accuracy of an impedance type measurement ("Z-type" apply I measure V) increases as impedance increases, and the accuracy of an admittance type measurement ("Y-type" : apply V measure I) increases as admittance increases, as illustrated below

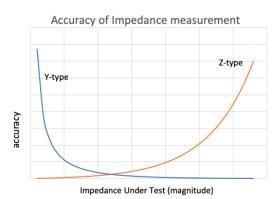


FIGURE 1.1: Impedance Measurement Accuracy

1.1.2 Steady state Measurements

The complex impedance measurement can be performed either in the sinusoidal steady state or by Fourier transform methods. This assignment is about a steady state measurement. For a sinusoidal steady state measurement a stimulus (voltage or current) is applied and a response (current or voltage) is measured in amplitude and phase. The sinusoidal steady state measurement can be performed either as a quadrature measurement or as a polar measurement. In the quadrature measurement the phase of the stimulus is known (or measured) and the response is measured in-phase and 90 degrees out of phase relative to the stimulus. This can be done by multiplying the response with the stimulus and a 90 degree out of phase delayed copy of the stimulus, and low pass filtered.

Phase measurements are also subject to some accuracy constraints. The accuracy of a relative phase measurement is maximum at 0 and 180 degrees, and degrades near 90 and 270 degrees, as illustrated below. It is often better to measure the phase difference to 90 degrees out of phase of the reference!

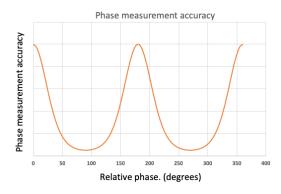


FIGURE 1.2: Phase Measurement Accuracy

In a polar measurement the amplitude of the response is measured, e.g. with an RMS detector, and then the phase with a phase detector or a phase-locked-loop.

1.2 Assignment

Design simulate, prototype and demonstrate a complex impedance measurement instrument which can measure complex impedance:

- Spot frequencies of 1kHz, 10kHz, 100kHz, (+optionally 1MHz)
- Impedance magnitudes from 10 Ohm to 1 M Ohm
- Impedance or admittance phase from -180 degrees to 180 degrees with 5 degrees accuracy.

These specifications cannot be achieved with a single range, either in magnitude or phase measurement.

The instrument should, therefore, be capable of switching between different modes of operation automatically under microcontroller control.

Controls for frequency, amplitudes, gains, etc. to allow range changes as necessary to achieve the stated range and specifications must be provided.

An ST Microelectronics NUCLEO F446RE microcontroller is recommended and supplied but any other microcontroller may be used. Dedicated GTA support is available to help you with the microcontroller subsystem.

Please note that marks will be awarded for effort and above all good and innovative design decisions justified by analysis and sound reasoning. A non-operational instrument, but one which is well engineered and well explained, may earn higher marks than an operational but poorly designed and inadequately explained and documented one.

1.2.1 Logistics

1.2.1.1 Groups

The work will be carried out in groups of 2 students. The group membership will be declared by email to me (c.papavas@imperial.ac.uk) by **Monday January 20st**. Students not members of a group by 20/1 should email me asking to be grouped.

1.2.1.2 Laboratory Facilities

All work will be in the 2nd year lab area on level 1. We have priority over the last three benches on the side closest to the windows. Power supplies, oscilloscopes, signal generators and digital multimeters are available, as well as RLC meters for reference and calibration. **Please avoid** using the Level 5 lab, which is reserved for final year projects.

1.2.1.3 Teaching Assistants

The GTAs for this course, and their primary areas of expertise, are as follows.

Cat Buizza	caterina.buizza11@imperial.ac.uk	Lab Work
Rodrigo Chacon-Quesada	r.chacon-quesada17@imperial.ac.uk	Lab Work
Daryl Ma (Lead)	jianwen.ma13@imperial.ac.uk	Printed Circuit Boards
Amir Nassibi	a.nassibi15@imperial.ac.uk	Microcontrollers

Surgeries in the lab with the GTAs will be announced.

1.2.1.4 Simulations

The Linear Technology LTSpice, is a free, favourite among professionals, simulator. LTSpice has a Wiki and a web users group with extensive resources, including tutorials. PSPICE is a licensed simulator available in the laboratory computers.

1.2.1.5 Prototyping

Circuit development will be carried out on breadboards. However, the row-to-row capacitance of these is high enough to severely limit the performance of an instrument made on breadboard. For this reason you will make your final device on a printed circuit board (PCB). PCBs will be 2 layer, plated through hole, and will be manufactured at Newbury Electronics PCB train Express (http://www.pcbtrain.co.uk). PCBs will be designed using any PCB design software you wish. The license-free Altium Circuit Maker software will be taught and supported by a GTA.

Each group will do their own assembly. Whenever possible please use through-hole components to make assembly easier. There will be one PCB design submission, due one week before the 2nd report:

• February 24th: PCB Design for manufacture

Boards will be available to groups for assembly one after submission. Submissions will be checked for errors, and may be returned to the groups for corrections before they are sent for fabrication.

1.2.1.6 Components

Each group will have a budget of £50 for components. Additionally to this budget each group will be allocated an ST NUCLEO F446RE microcontroller and a breadboard. Components (preferably from RS and Farnell for rapid delivery) will be ordered by groups directly through the Department Stores, and charged to "UG teaching 3rd year, E302".

A spreadsheet with orders will be submitted with the final report. Budget overruns without prior approval will incur a marks penalty.

1.2.1.7 Assessment

There will be three reports and one interview. The following is a list of course deadlines:

- 1. Top level design, concept (25%). Due Monday 3/2 9AM.
- 2. Design Report (25%). Due Monday 2/3 9AM.
- 3. Demo / Interview (25%) during last week of Term 19-20/3 (To be arranged)
- 4. Final Report (25%). Due by 5pm on 20/3

1.3 Coursework Assignment 1: Initial Design (25% of Term Marks)

A brief report of up to four pages (including figures), handwritten-scanned or typeset with 10pt minimum font, is due on Blackboard by **Monday February 3rd by 9AM**.

This report includes a few comprehension questions plus:

- Design overview
- Operating Principle
- Modes of operation
- Accuracy estimates
- System block diagram
- Analogue Interface circuit schematic design
- Scanned handwritten submission will be accepted
- The 4 page limit includes all figures and tables.
- No appendices will be accepted. Any appendices submitted will be ignored.

1.4 Coursework Assignment 2 (25% of Term Marks)

A brief report of up to six pages (including figures), handwritten-scanned or typeset with 10pt minimum font, is due on Blackboard by Monday March 2nd by 9AM.

This report includes the comprehension questions plus:

- Final Schematic diagrams.
- Final PCB design, pictures of top and bottom metals
- High level description of microcontroller code.
- Revised operation modes, accuracy estimates.

A zip file containing the PCB manufacturing files (Gerber files) plus PDFs of the schematic and the metal layers must be submitted a week earlier, i.e. on Monday February 24, 9AM.

- Scanned handwritten submissions will be accepted
- The six page limit includes all figures and tables.
- No appendices will be accepted. Any appendices submitted will be ignored.

1.5 Demo-Interview (25% of Term Marks)

A group interview with the Course Leader and a GTA will be scheduled at a convenient time during the last week of term, between Thursday March 19th and Friday March 20th. The interviews will be scheduled by electronic signup on a first come, first serve basis.

The interview will last half an hour.

During the interview you will be asked to demonstrate the operation of your instrument on 2-3 unknown devices supplied by the examiners.

Agenda:

- Describe your instrument
- Demonstrate operation with your own DUT

- Answer general comprehension questions.
- Measure two unknown DUTs

Marks will be awarded for:

- Smooth operation of the instrument
- Accuracy of determining the DUT impedance.

1.6 Final Report (25% of Term Marks)

A final report detailing the design, any simulations, and measurements is due by 5pm on Friday March 20th.

The report must be at most ten pages long including figures and diagrams, It may be handwritten- scanned or typeset with 10pt minimum font.

The report must contain:

- Final schematic diagrams if changed since 2nd report
- Photograph of the prototype.
- List of input and output signals of the instrument.
- Specifications achieved
- Simulations (if available)
- Bill of materials and total cost of orders submitted.
- Graphs of measurements covering the range achieved.
- Algorithm or pseudocode for calibration, self calibration, automation.
- Group Member roles and contributions

This report should be up to TEN pages plus a pictures of the schematic, and the PCB.

- Scanned handwritten submissions will be accepted
- The ten page limit includes all figures and tables.
- No appendices will be accepted. Any appendices submitted will be ignored.

Chapter 2

PCB Implementation

2.1 Information

2.1.1 Aim

Learn the full process of designing a printed circuit board with Altium Circuitmaker.

2.1.2 Guides

There are a few helpful guides that will be useful:

- 1. CircuitMaker Documentation¹
- 2. CitcuitMaker $FAQs^2$
- 3. The Circuit Designer's Companion by Tim Williams

Additionally, you can approach your GTAs with any questions. For computer related issues, you can contact the Computer Support Group.

 $^{^{1}} https://documentation.circuitmaker.com/display/CMAK/From+Idea+to+Manufacture++Driving+a+PCB+Design+through+CircuitMaker$

²https://documentation.circuitmaker.com/display/CMAK/CircuitMaker+-+((FAQs))

2.2 Project Background

2.2.1 Prototyping Process

In this exercise, the aim is to design a prototype that will fulfill its specifications, likely under fixed laboratory conditions. There can also be circuit design for production-ready circuits, but we will not cover that here.

The process for integrated circuit design generally follows this format:

- 1. Gathering Specifications/Requirements for Device
- 2. Determine components capable of meeting these requirements
- 3. Simulation of theoretical circuit
- 4. Printed Circuit Board Implementation
- 5. Testing and Validation
- 6. Reiteration for new improved Device

These set of notes would cover only the Printed Circuit Board implementation area, and mainly involve schematic entry, PCB layout, and the relevant design rules checks.

2.2.2 Circuit to be Implemented

2.2.2.1 Conditions

There will be some fixed conditions:

- 1. Control unit would be the STM32 Nucleo-64 Development Board.³
- 2. Only Through-Hole components.
- 3. Two-sided board with vias.
- 4. Board Size of 100mm x 100mm
- 5. Use components from Linear Technology and Analog Devices

These conditions should be followed to the best of your ability. In the event that you would like to use other choices, approach the GTAs to let us know. The remaining circuit would be left to your creativity.

³https://www.st.com/en/evaluation-tools/nucleo-f302r8.html

2.2.2.2 Demonstration

To demonstrate an example, the circuit to be implemented would consist of the STM32 Nucleo-64 Development Board, with dual in-line package sockets to plug the board into the PCB. Following on, two external LEDs would be used to provide visual indicators, and a potentiometer would be used to provide a variable voltage input to be read on one of the pins.

Chapter 3

Schematic Layout

3.1 Learning Objectives

- How to set up CircuitMaker
- How to add new schematics and components

3.2 Setting Up Altium CircuitMaker

3.2.1 Registration

First, you'll have to set up your account. Sign up for an account through this link ¹. Once that is done, go ahead and login. Start the CircuitMaker app on windows, and the login page should show up as shown in Fig. 3.1. Sign In.

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				USER NAME					
				Email					
				PASSWORD					
				Password					
				Remember N	te Forgot passwo	ord?			
				Sign In					
		¢							,
lenages									_

FIGURE 3.1: Login Screen

¹https://workspace.circuitmaker.com/Account/SignUp

3.2.2 Starting a New Project

To create a new project, click on Add New Project in the home screen, or <u>File \rightarrow New Project</u>. In the window that appears as shown in Fig. 3.2, type your group name in the name field, and the members names in the description. Set the privacy settings to sandbox.² Click Ok. On the next Edit Project screen, click Save.

<group name=""></group>			
Project Name field	is invalid		
Public O	Sandbox		
Group Members			

FIGURE 3.2: New Project Screen

3.3 Schematic Layout

3.3.1 Add New Schematic

You will see a Projects Panel appear as shown in Fig. 3.3. To add a schematic to your project, click on <u>Home \rightarrow Projects \rightarrow Add new Schematic</u>. As this schematic will contain the control unit, enter the schematic sheet name as *Control_Unit*, and click ok.

3.3.2 Adding Components

CircuitMaker has an advantage of being closely tied to an online component search engine database(Octopart). That means commonly used components would likely have their schematics and PCB footprints already created and stored on the cloud. However, **always check that the schematic matches the datasheet of the chosen component.** There are multiple revisions of a single component, and you will never know if a pin is switched on a new revision. Checking and making sure that the schematic is correct now would minimise mistakes later.

 $^{^{2}}$ This makes the design private, and only allows people given permission rights to view or edit the project.

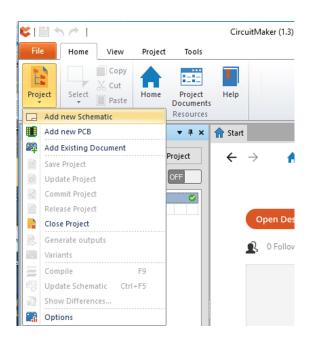


FIGURE 3.3: Projects Panel

To open the library panel, click on <u>View</u> \rightarrow <u>Libraries</u> as shown in Fig. 3.4. Change the library to Octopart, and type in Nucleo-64. Select <u>STM32F446RET6 Microcontroller</u>, and click Place. As you move your mouse cursor over the blank schematic, you should observe the schematic model of the STM32 Nucleo-64 Evaluation Board. Click to Place.

Octopart		~
Nucleo-64		
	Categories	`
4	STMJcroelectronics NUCLEO-F448RE STMJ2F448RE16 Microcontoller Development Board 512KB Flash Win 7/Win 8/Win Vista/Win XP Core Architecture ABM: Core Sub-Architecture: Corter-M4; Lead-Free Status: Lead Free; Lifecycle Status: Active; Number of Bits: 32; Noifs: Compliant	
Ċ	STMicroelectronics NUCLEO-F411RE STM32F411RE16 Microcontroller Development Board 512KB Flash Win 7/Win 8/Win Vista/Win XP Cora Architecture ARM: Cora Sub-Architecture: Cortex-Mic Lead Free; Lifecycle Status: Pre-Release; Number of Bits: 32; REACH SVHC Compliance: No SVHC; RoHS: Compliant	
	STMicroelectronics NUCLEO-F401RE STM32F401RE Embedded Nucleo STM32F4 MCU 32-Bit ARM Cortex-M3 Evaluation Board	
	PLACE BUILD	

FIGURE 3.4: Adding Components

Repeat the following for the additional components:

- 2 x 220R through-hole resistors
- 2 x LED
- 1 x potentiometer

You are free to choose any components you like, as long as they abide by the conditions given beforehand. You should have something like this as shown in Fig. 3.5.

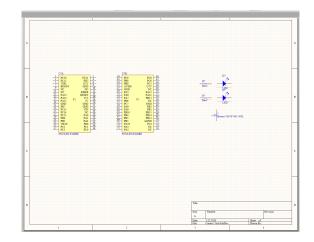


FIGURE 3.5: Components on Schematic

3.3.3 Wiring and Arrangement

It is good practice to have a clean schematic - Having multiple wires criss-crossing, or components that should be near each other placed far away should be avoided as much as possible. As circuits increase in complexity, having a clean schematic would improve the speed of analysis and help aid good design.

Let's begin by arranging the components where they should be. First, the 2 LEDs and their resistors would be placed near PA0 and PA1. These are chosen as PA0 corresponds to I/O PA0 of the microcontroller, and PA1 corresponds to I/O PA1.Remember these ports, as you would be using them later to program the pins in the correct locations.

Next, place the potentiometer next to *PA3*. This is chosen as *PA3* corresponds to the Analog to Digital Converter (ADC123IN3) on the microcontroller.Fig. 3.6 describes the entire pin out diagram of the Nucleo-64 evaluation board.

Finally, add in ground and power ports. To add the ground port, <u>Right Click</u> \rightarrow <u>Place</u> \rightarrow <u>Place GND power port</u> or use the shortcut <u>Z</u>. For a power port, <u>Right Click</u> \rightarrow <u>Place</u> \rightarrow <u>Place VCC power port or use the shortcut <u>V</u>.</u>

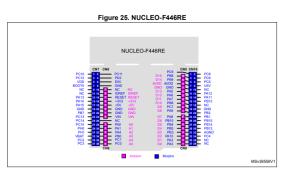


FIGURE 3.6: Pin Out of Nucleo-64 Development Board

As the development board would have two means of being powered, either through the USB connector located on the board, or through the E5V, 3V3 or VIN pins located on the board, we should clearly demarcate the different power supplies. Additionally, the development board supplies its own 3V3 from pin 12 or 16 and 5V from pin 18 supply when powered from USB.

Connect a power port named <u> $3V3_OUT$ </u> to the 3V3 pin. Likewise, do the same for the E5V pin with a power port named <u> $E5V_EXT$ </u>.

Once the components have been arranged neatly, begin wiring the circuit up using the shortcut W. Once done, place a directive for no Electrical Rules Check(ERC) on pins of the development board that will not be used. This will allow any errors that may flag up from the ERC due to there not being any pins connected being removed. To do so, go to Right Click \rightarrow Place \rightarrow Directives \rightarrow Generic No ERC.

3.3.4 Editing Properties

Lastly, to edit the components individually, Right Click on the component and go to <u>Properties</u>. A window as shown in Fig. 3.7 should appear. In this window, edit the comment field to reflect the values of the passive components you are using. A useful trick to check the component is also in the preview window, where you can view the 3D model of the component you are using. Hold shift and right click on the figure in the preview window to view the component from different angles. You can also click on the hammer logo on the bottom left to change the view to a 2D view. This allows you to take a look at the footprint of the component as shown in Fig. 3.8.

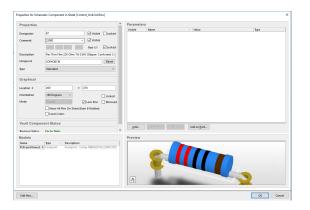


FIGURE 3.7: Properties Window

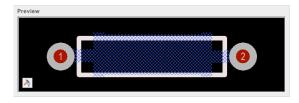


FIGURE 3.8: 2D Image

3.3.5 Net Labels

Net labels are helpful to determine where each wire leads to. This has an added advantage later in the PCB layout, and having a name for each wire allows you to differentiate them correctly. To add net labels, use the shortcut \underline{N} and add it to the wires you would like to label.

Once that is done, finish off by annotating the components. This can be done by $\underline{\text{Tools}} \rightarrow \text{Annotate} \rightarrow \text{Annotate Schematics Quietly}$. The finalised schematic can be seen in Fig. 3.9.

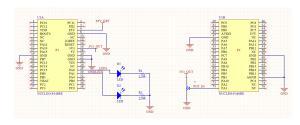


FIGURE 3.9: Completed Schematic

3.3.6 Electrical Rules Check

To begin the electrical rules check, you would have to save and commit the project first. Do this by going to $\underline{\text{Project}} \rightarrow \underline{\text{Save Project}}$, and then $\underline{\text{Project}} \rightarrow \underline{\text{Commit Project}}$. Additionally, go to $\underline{\text{View}} \rightarrow \underline{\text{Messages}}$ to observe any error messages that may pop up during compilation. Finally, use the shortcut <u>F9</u> to compile the project.

An example of an error is displayed here in 3.10. If errors occur, check and see if they are critical or non-critical errors.

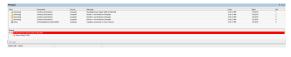


FIGURE 3.10: Error Message

Once your project has compiled successfully, you are ready to begin with the PCB layout.

Chapter 4

PCB Layout

4.1 Learning Objectives

- How to set up the PCB Layout before design
- How to transfer the schematic to layout
- How to route manually and automatically
- How to utilise polygon pours
- How to apply silkscreening
- How to perform the Design Rules Check
- How to obtain the manufacturing file Outputs

4.2 Setting up the PCB layout

First, we'll have to add a new .CMPcbDoc to the project. Go to <u>Home \rightarrow Add New PCB</u> and enter the new file name as the same name as your group name. Once done, you should observe a black board layout with a white dotted line demarcating the edges.

4.2.1 Units and Board Origin

Before we begin, we will change the grid size from imperial units to metric. This helps obtain a better feel for the board size, as we are now dealing with the physical representation of the PCB. Go to Home \rightarrow Board \rightarrow Board Options and change the measurement units from Imperial to Metric as shown in Fig.4.2.

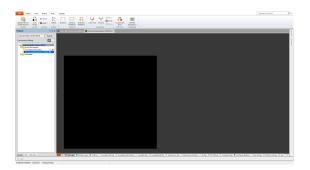


FIGURE 4.1: New PCB Document

 Image: The state of t

FIGURE 4.2: Changing Setting to Metric

Next, set the origin to the bottom left point of the board cutout. Go to <u>Home \rightarrow Grids and units</u> \rightarrow Origin & Jumps \rightarrow Set and click on the point where you want your origin to be. The bottom left corner is chosen here and all component locations would now be referred to from this point.

4.2.2 Reshaping Board

The default board shape is larger than what is required. Since the size of the components are already known, we will reshape the board shape to a smaller size to minimise space.¹ Let's redefine the board size to 50x80mm. First, let's change the snap grid size to 2.5mm to make it easier to mark out the edges. Go to Home \rightarrow Grids and Units \rightarrow Snap Grid, and change the field to 2.5mm.

Next, go to Home \rightarrow Board Shape \rightarrow Redefine Board Shape. This begins off from the origin, and you can set the board shape by clicking on the other 3 corners that you would like as seen in Fig. 4.3. Use the X and Y coordinates at the bottom left of the window to help you define the distances correctly. Fig. 4.4 displays the new board shape.

4.2.3 Layer Stack Manager

Go to <u>Home \rightarrow Board \rightarrow Layer Stack Manager</u> to observe the physical layers of the PCB as shown in Fig. 4.5. The default settings should correspond to a two layer board, with a top and bottom signal layer between a FR-4 dielectric core. We will not go into too much detail here, but note that you can change the number of layers on the board as you see fit.

¹In addition to this, most PCB manufacturers charge by the size of the PCB. Having a smaller PCB essentially also equates to a less expensive one.

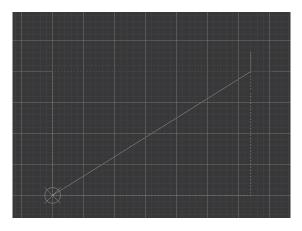


FIGURE 4.3: Changing Board Shape

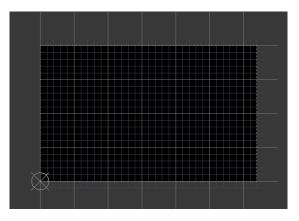


FIGURE 4.4: Board Shape Complete

Save Load Presets	• 🗆 3D			4) (°4	M	Custom Custom	~
	Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm
	Top Overlay	Overlay					
	Top Solder	Solder Mask/Co	Surface Material	0.0254	Solder Resist	3.5	
	Top Layer	Signal	Copper	0.03556			
	Dielectric 1	Dielectric	Core	1.524	FR-4	4.6	
	Bottom Layer	Signal	Copper	0.03556			
	Bottom Solder	Solder Mask/Co	Surface Material	0.0254	Solder Resist	3.5	
	Bottom Overlay	Overlay					
	<						>

FIGURE 4.5: Layer Stack Manager

Next, we will have to set up the design rules for the project. Design rules here are the rules that determine the minimum clearance between tracks, how small the via diameter can go, or the minimum angle between tracks allowed. These are generally determined by the manufacturer, whose tooling machines have a physical limit to their performance. Before starting any design, always go through the PCB manufacturer's design specifications before routing the components. For this project, we will be going with PCB train specifications². Change the following parameters:

- 1. Manufacturing Hole Size
- 2. Solder Mask Expansion
- 3. Minimum Routing Width

Fig. 4.6, 4.7 and 4.8 give an impression of the values chosen for this project. However, check through the specifications and understand the rationale behind these chosen values.

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	Minimum 0.3mm Maximum 2.54mm				
Buie Wizard		ОК	Cancel	Apph	y

FIGURE 4.6: Via width change

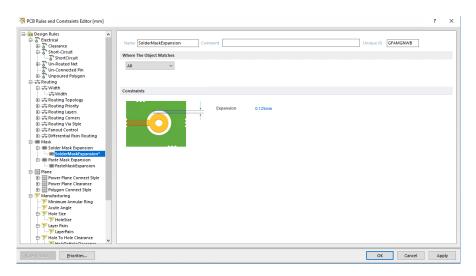


FIGURE 4.7: Solder Mask change

Once this is done, we can finally move on to bringing the components into the layout editor.

 $^{^{2}} https://www.pcbtrain.co.uk/resources/pcb-technical-capability$

Design Rules								
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E S Unpoured Polygon								
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🕀 🖧 Routing Layers	Min Width 0.2	Max Width 0.254mm						
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FIGURE 4.8: Minimum Track Width

4.3 Bringing Components In

To import the schematic capture components to the PCB document, first click on the Control_Unit.SchDoc in the Projects Panel. From there, go to <u>Home \rightarrow Project \rightarrow </u><u>Update PCB Document in <Group Name>.PrjPcb</u>. An Engineering Change Order(ECO) window should appear as shown in Fig. 4.9. Click on validate changes, then execute changes. Validate changes flags any modifications done to the schematic, and allows you to observe any changes in the wiring if it has been done. Executing the change performs this change in the PCB layout itself.

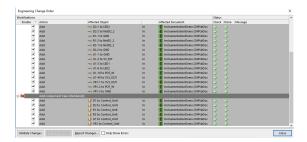


FIGURE 4.9: Engineering Change Order

Navigate back to the PCB layout editor, where you should now observe the components as shown in Fig.4.10. You can then use the shortcut $\underline{3}$ or $\underline{2}$ to toggle between 2D view modes and 3D view modes respectively. Note that the 3D view mode effectively acts as a viewer, but to ensure grid locations are met, components should mainly be edited in the 2D view mode.

Similarly, begin by arranging the components to their ideal locations. An example would be for external wire connections to be connected to the edge of the board. In this case, the USB cable supplying the power should be as close to the edge of the board

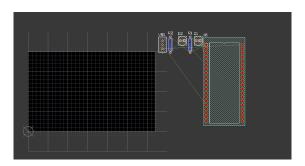


FIGURE 4.10: Components added to PCB layout

as possible. Change the snap grid to 0.5mm, and use shortcuts such as <u>spacebar</u> while editing the components to rotate them.

There are small lines linking the pins together. These lines are termed "Rats Nest". These lines should be kept as short as possible to minimise routing lengths.

4.4 Routing

There are two methods of routing - Automatic or manual. Automatic leaves the control of the routing paths to the software itself, and churns out routes. This gives the designer the ability to save design time at a cost - these paths may sometimes not be the most efficient route to the pin, or the software does not have an idea of the best board layout management practices. Sometimes, autorouting leaves the designer with more work to do simply correcting the non-optimised routes. Hence, manual routing also gives a choice of absolute control to the designer for the most efficient and optimised layout as per the designer's wishes.

4.4.1 Autorouting

For a simple board in this demonstration, autorouting would serve the purpose as there are few enough routes for the designer to check.

For autorouting, go to $\underline{\text{Tools}} \rightarrow \text{Autoroute} \rightarrow \text{All}$. In the pop up window that appears, leave the default 2 layer board strategy as shown in Fig. 4.11. Then click on Route All to let the autorouter do so. Fig.4.12 displays the board layout after autorouting has completed.

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FIGURE 4.11: Autorouting Setup

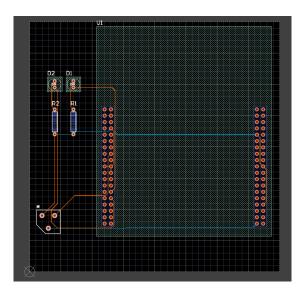


FIGURE 4.12: After Autorouting

4.4.2 Manual routing

Now, to demonstrate manual routing, two additional vias for the 5V external supply will be added. These allows for use cases when the USB input is not available.

4.4.2.1 Editing PCB Component Properties using Filter and Editor

Go to <u>Home \rightarrow Pad</u> and click to add two pads, preferably at the edge of the board. Next, we will edit the properties of these two pads to a size that will be easy to connect external wires from a power supply to. One useful tool to use is the filter tool. This allows the designer to filter out components in the design that should be edited, and allows you to edit these components at the same time.

Go to <u>View</u> \rightarrow <u>Filter</u>, and select <u>Free</u> for Groups and <u>Pad</u> for Objects as illustrated in Fig. 4.13. This will highlight the two pads you have just added, as they have not been connected to any other nets yet. Select these two pads.



FIGURE 4.13: PCB Filter Tool

Now, navigate to the PCB panel on the bottom left of the screen as shown in Fig. 4.14. Change the field to Hole Size Editor at the top, and change the Condition Selection to Show selected Objects. This should give you the 2 holes in the middle panel. Now, change the sizes from 0.762mm to 1mm by typing into the Hole Size field. Select yes on the Confirm hole size modification window. This will edit the two pads at the same time, and is a useful tool for editing large numbers of components at once.

Next, we will assign nets to these pads. At the moment, these pads are not connected(NC), and are given arbitrary numbers. Change the net under properties to $5V_EXT$. For the other pad, change the net to GND as shown in Fig. 4.15.

The rats nest should pop up, indicating the closest 5V_EXT net and GND net to the pads. To manually route them, use the shortcut $\underline{\mathbf{R}}$ and click on the pads. Doing so would highlight the net that is selected, allowing the designer to view the best possible link available.

To change layers, use the tabs at the bottom of the screen. To route to the bottom layer, select the bottom layer tab at the bottom of the screen, and route as normal.

This process of adding pads can also be applied for adding testpoints. With more complicated circuits, adding more testpoints for the prototype is ideal to improve the speed and ease of testing. Having a pad to apply a probe and another pad to apply the GND to is much simpler than having to solder wires to make the connections.

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FIGURE 4.14: PCB Editor Tool

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FIGURE 4.15: Changing the Net

4.5 Polygon Pours

Polygons is the term given to large copper areas used to provide a common net. Usually, the ground or power net is used as the polygon pour, for signal noise reduction or heat dissipation reasons. Go to Home \rightarrow Pour \rightarrow polygon Pour.

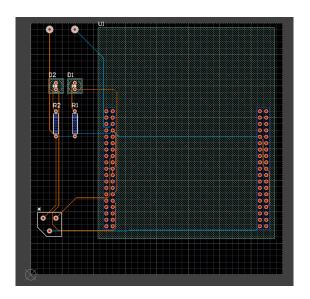


FIGURE 4.16: Bottom Layer Routing

On the Polygon Pour screen, we will add the polygon. Change the Name to <u>Top Layer - GND</u>, and the Layer to <u>Top Layer</u> as shown in Fig. 4.17. For the Connect to Net option, set it to GND. Click Ok.

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FIGURE 4.17: Polygon Pour Setup

Select the four corners for the polygon pour, and then press Esc to end the process. The polygon pour should automatically fill the gaps in the board a shown in Fig. 4.18.

Note in Fig. 4.18 that there's a block of polygon that is not connected to any net. This is what is termed an island. To get rid of these, select the polygon, and right click to access its properties. Change the *Remove Islands Less than ifield*; (sq.mms) in Area

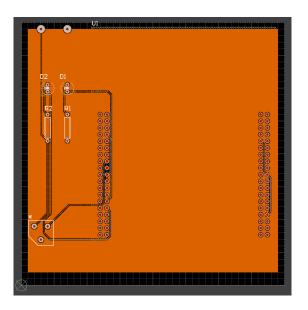


FIGURE 4.18: Polygon Pour Result

field to 10 as shown in . Click ok, and proceed to repour. This should remove the islands as shown in Fig. 4.20.

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FIGURE 4.19: Removing islands

4.6 Silkscreening

The silkscreen is the visual interface of the board to the user. A good silkscreen would make the board easy to understand and use, and reduces any mistakes after the board ends up in the hands of a designer. Be as artistic as you can, and enjoy the process.

Navigate the bottom tabs to the Top Overlay. Go to <u>Home \rightarrow Place \rightarrow Text to add the text in. Now, you can add in any text you want. You can vary the size of the font in properties, or change the font type. This is up to your own discretion.</u>

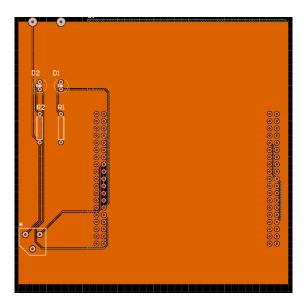


FIGURE 4.20: Polygon Pour after Islands Removed

4.7 Outline Layer

To allow the manufacturer to know the size of your PCB, it is integral to include an outline layer. Without this outline layer, the designed PCB would not be accepted for manufacturing.

To include an outline layer, click on the outline tab at the bottom of the screen. Next, draw a line using the <u>Place \rightarrow Line</u> tool around the board outline as shown in Fig. 4.21.

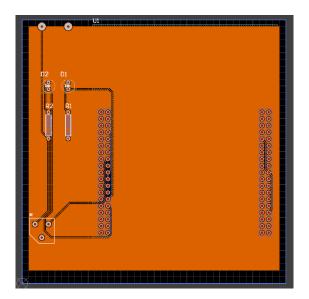


FIGURE 4.21: Board Outline

4.8 Design Rule Check

Once you are ready to proceed, run the Design rules check(DRC) to ensure that the board layout meets the required standards. Go to $\underline{\text{Outputs}} \rightarrow \text{Reports} \rightarrow \text{Design Rule Check}$. As we have set up the rules previously, go ahead and Run Design Rule Check.

D		
in Pepart Options ∰Peter Context Telefactual 2 Execution 1 Anoutacuing 1 An	DRC Report Options Create Report File Create Report File Create Violations Subject Details Subject Details Viving Storming Corper Report Buildinger Parks with 0 size Hole Store Hole Store Hole Split Report BCR Report Options Report Details Report Report Detail Corper larger than Report Starved Thermals with less that Store Report Starved Thermals with less that Store Report Starved Thermals with less that	
	NOTE: To generate Report File you must save your PCB document first. To speed the process of rule checking enable only the rules that are required for the task being performed. Note: Options are only enabled when corresponding rules have been defined. Design-Rules dialog to be able to test for a particular rule type.	

FIGURE 4.22: DRC Check

A DRC report should appear as shown in Fig. 4.23. Understand the errors, and fix them. For the warnings, try to minimise them as much as possible.

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Design Rule	e Verification Report						
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Summary							
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FIGURE 4.23: DRC Report

4.9 Manufacturing File Outputs

There are a number of outputs you can generate. Assembly Outputs refer to files used by a pick and place machine for auto-assembly. Documentation Outputs provide the schematics and PCB drawings for analysis. Fabrication outputs provide the files and guides for the drilling required for the pad locations. Finally, **Report Outputs** provide the rules check, as well as the Bill of Materials(BOM) regarding the components used on the board.

4.9.1 Configuring Gerber Files

In this project, we would need to obtain the Manufacturing Outputs, which take the form of Gerber files. First, Go to <u>Outputs</u> \rightarrow <u>Gerber</u>. Under General, change the units to Millimeters, and the Format to 4:3.

General	Layers Drill Drawing Apertures	Advanced	
	Specify the units and format to This controls the units (inches o after the decimal point.	be used in the output files. r millimeters), and the number of digits before an	ıd
	Units	Format	
	Oinches	• 4:2	
	Millimeters	O 4:3	
		0 4:4	
	The 4:2 format has a 0.01 mm re 0.1 um resolution.	the requirements of your Project. solution, 4:3 has a 1 um resolution, and 4:4 has a er resolutions you should check that the PCB mat.	
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	The 4:2 format has a 0.01 mm re 0.1 um resolution. If you are using one of the higi	solution, 4:3 has a 1 um resolution, and 4:4 has a er resolutions you should check that the PCB	
	The 4:2 format has a 0.01 mm re 0.1 um resolution. If you are using one of the higi	solution, 4:3 has a 1 um resolution, and 4:4 has a er resolutions you should check that the PCB	

FIGURE 4.24: Gerber Setup for Millimeters and Resolution

Under the Layers tab, select Plot Layers, and click used on.

Gerber Setup				×
General Layers Drill Drawing	Apertures A	dvar	nced Mechanical Layers(s) to Add to A	All Plots
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<u>P</u> lot Layers ▼ <u>M</u> irror Layer All On All Off	rs ▼ □ įn	ICluc	le unconnected mid-layer pads	
Used On			ОК	Cancel

FIGURE 4.25: Gerber Setup for Layers

Finally, go to advanced tab, and check the *Reference to relative origin* circle. Once this is done, click OK.

eneral	Layers	Drill Drawing	Apertures	Advanced	
Film Si	ze			Leading/Trailing Zeroes	
<u>X</u> (ho	rizontal)	508mm		○ Keep leading and trailing zero	
<u>¥</u> (ver	tical)	406.4mm		Suppress leading zeroes	
Bord	er size	25.4mm		○ Suppress <u>t</u> railing zeroes	
Apertu	re Match	ing Tolerances		Position on Film	
Plus		0.0001mm		O Reference to absolute origin	
Mi <u>n</u> u	s	0.0001mm		Reference to relative origin	
				○ <u>C</u> enter on film	
Batch	Mode			Plotter Type	
٥	<u>e</u> parate 1	file per layer		Unsorted (raster)	
OP	anelize li	ayers		○ Sorted (vector)	
Other		erture change		Optimize change location command	
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	-	ons for octago	nal nadr	Generate DAC Rules export the (.Ru	-
	oc polyg	ons to ottago	nar pada		

FIGURE 4.26: Gerber Setup for Relative Origin

4.9.2 Configuring Output Files

Go to <u>Project</u> \rightarrow <u>Generate Outputs</u>. Commit and save your project as required. Check the Schematic Prints, Board Information, Gerber Files and NC Drill Files for the outputs, and Generate. This should produce a zip file. Download it.

Outputers	Configure	Page Setup	Status	
🗁 ВОМ				
📴 Bill of Materials	Configure	Page setup		
🗁 Documentation				
🛃 Schematic Prints	Configure	Page setup		~
PCB Prints	Configure	Page setup		
🛃 PCB 3D Print	Configure	Page setup		
Board Information				•
E Fabrication				
🜉 Gerber Files	Configure			×
NC Drill Files	Configure			¥
ODB++ Files	Configure			L
Report Board Stack	Configure			
Assembly				
Generates pick and pla				Ļ
Assembly Drawings	Configure	Page setup		L
Calidation				
🛃 Design Rules Check		Page setup		Ļ
Electrical Rules Check	Configure	Page setup		
Export				_
Export STEP	Configure			

FIGURE 4.27: Generate the output files

4.9.3 One Last Check

Use a gerber viewer to see if the files has exported correctly. You can do this by using an online $tool^3$ to see if the drill holes correspond correctly to your project.

For the PCB submission, you will be sending a zip file containing both the Gerbers and NC drill files. This file can be uploaded onto the website above, from which you can observe what the manufacturer would see.

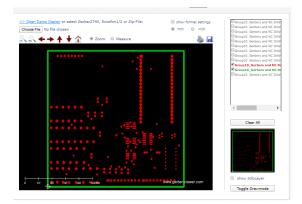


FIGURE 4.28: Online Gerber Viewer

Fig. 4.28 displays the online gerber viewer tool, from which there are a number of files shown on the right. These files correspond to the various layers of the PCB, as well as the drill locations as required.

As mentioned previously, ensure that 3 things are included before submission:

- 1. Outline Layer displaying the board shape (shown in green)
- 2. Gerber files with layers required
- 3. NC drill files

Remember that if these files are not included, your PCBs would take much longer to manufacture, affecting the time you have for testing.

³http://www.gerber-viewer.com/