2021 IEEE International Symposium on Medical Measurements and Applications (MeMeA) | 978-1-6654-1914-7/20/$31.00 ©2021 IEEE | DOI: 10.1109/MeMeA52024.2021.9478708

Multiple Input, Single Output Frequency Mixing Communication Technique for Low Power Data Transmission

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***Abstract*—The paradigm of Internet of Things (IoT) has revolutionised the field of human health monitoring. Recent research works outline an ever growing interest in the development of miniaturized fully functioning devices, where optimization strategies in terms of size, power consumption and data transmission capabilities represents the main requirements as well as the biggest challenges at the design stage. In this paper we provide an analysis into a data transmission method based on digital mixing for combining multiple inputs channels into a single output. We first demonstrate that the sources of the error generated in the output stream are the frequency ratio of the input signals and their relative phase shift. With the results from the simulations, we demonstrate that the error performed on the lower frequency information in the mixed signal has a trend which is exponentially decreasing with the input frequency ratio. Additionally, we prove that the relative phase shift of the input signals may significantly impact the error towards lower input frequency ratios. Afterwards, we analyze the system power consumption, and we demonstrate that the power trend is linear with the input frequency ratio. Lastly, we discuss the error performance versus power trade-off of the system, which is helpful for the design of the input frequency levels for a specific target application.**

***Index Terms*—Multiple input, Single output Data Transmission; Digital Mixing; Error Performance; Functional Simulation; Power Consumption; CMOS**

I. Introduction

The prospect of utilising Internet of Things (IoT) devices exists for an abundance of systems [1]. The overarching aim is to connect all devices to the Internet and communicate with each other with minimum human intervention [2]. Recent development into the possible implementation of IoT devices for biomedical purposes have recently gathered pace, with Carrara et al. [3] raising the possibility of developing wireless miniaturized CMOS Bioelectronics for the detection of cancer cells.

To achieve the possibility of developing such an implantable device, its size, power consumption and data transmission capability must be optimised for biomedical purposes [4]. This requires the integration of wireless data transmission, which is advantageous for transmissions from areas that are inaccessible with wires. Additionally, since these devices are often expected to continuously sense, collect, and transmit data, the need for frequent recharging is troublesome, especially in health applications such as aged-care, where the users may easily forget to recharge wearables [7].

To this end, the choice of a suitable communication protocol becomes a crucial task, since the resource constraints of such devices make the development of low-power wireless systems more "error-prone", especially when multiple information sources have to be transmitted simultaneously [5] [6].

This paper presents an analysis for the application of a data transmission method based on digital mixing, which transmits the two data streams with a single output. Specifically, we examine it in terms of error performance and power consumption and investigate the main sources of error and energy consumption to provide some system level metrics in regards to the potential trade-offs. An example hardware implementation consists of a D flip-flop used in a divide-by-two counter set-up with asynchronous active-low reset as illustrated in Fig. 1. The input signals are continuous time digital signals produced by dedicated sensing nodes, and the information they carry is embedded in their frequency (or period) variation. The output produced by the mixer transmits simultaneously the information of both the source signals. The reconstruction of the information at the receiver side will be based on frequency measurement and the specific method employed, as well as the architecture, will depend on the application. Furthermore, this communication method supports wireless power and data transfer, as outlined in design by Ma et al. [9], which represents the first example of an application of the proposed method. This system, which is termed as "DAPPER", is an analog front-end circuit that performs concurrent potentiometry and amperometry sensing. With digital mixing, which allows to combine the two readings, the system produces a single output.

The concept of digital mixing and the analysis of D flip-flops as a differential mixer has been discussed several times in literature [8], and the study of the error performance has been achieved with time-base analysis or test methodologies based on real hardware devices. However, digital mixing as a method to enable multiple signal transmission for low power wireless communication has not been explored in greater depth, in particular the types of errors arising from varying input frequencies. Additionally, a test methodology that is

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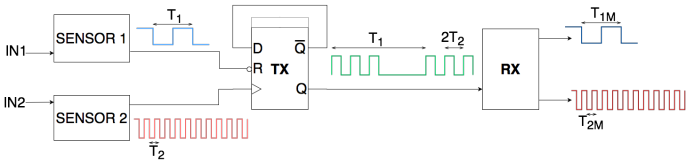

Fig. 1. Conceptual architecture of the communication protocol based on digital mixing. Two square waves are generated by dedicated sensing nodes and sent to the mixer. The D flip-flop is used in a divide-by-two counter set-up, demonstrating one example of a digital mixing implementation. The latched D flip-flop serves to ensure the output duty cycle always remains at 50%, which simplifies the demodulation process at the receiver end. The mixed signal can be transmitted through a wireless channel and the receiver reconstructs the original information from the mixed signal.

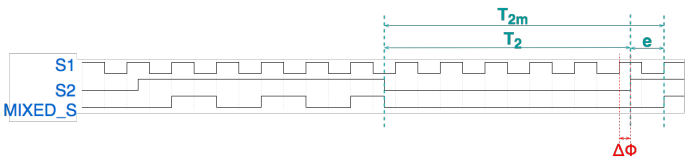

Fig. 2. Timing diagram of the signals involved in the mixing process and related errors on the output signal. $\Delta\phi$ is the relative phase shift of the input signals (S_1 and S_2). T_2 is the period of the signal with the lower frequency (i.e. S_2). T_{2_m} is the period of S_2 in the mixed signal, that is characterized by a certain error e with respect to the original period T_2, and that arises from the input frequency ratio and from $\Delta\phi$.

independent of the timing/technology/implementation details for the analysis of the error performance in this field is yet to be achieved.

The proposed method in [9] also showcases the limit of signal mixing in terms of error and the resulting constraints on the frequency ratio of the input signals have been demonstrated. In particular, the smaller the frequency ratio, the higher the error on the lower frequency information in the mixed signal. This research will build upon this by examining in greater detail the error performance of the system, with the aid of a particular test methodology. The final power analysis will provide the means to investigate the power-error trade-offs and to find the optimum operating conditions for the digital mixer.

The rest of the paper is organised as follows. In Section II, the test method for the error analysis is described. Section III is dedicated to the results of the simulation and the analysis of the system error performance. The power-error trade off is discussed in Section IV, followed by the conclusion and future work.

II. Test Method

The test method serves to analyse and characterise the main sources of error, as well as an estimation of their impact on the system performance. This error arises because of the loss of information in the output signal with the mixing process. The study of the sources of error can be achieved by observing the output characteristics of the D flip-flop.

Fig. 2 shows the possible timing diagram of the signal mixing and highlights the two main sources of error: (1) the frequency ratio of the two input signals (S_1 and S_2) and (2) the relative phase shift ($\Delta\phi$). In the mixed signal (Mixed_S), errors occur for both the input frequencies. Fortunately, for the higher frequency signal the large amount of pulses sampled compensates for the error. In contrast, the relatively low number of pulses on the lower frequency signal means any error would inherently mean the information will be lost. The error arising from the signal at the lower frequency (S2 in Fig. 2) can be evaluated in relative terms as:

$$e_{r_{T_2\%}} = \left| \frac{T_2 - T_{2_m}}{T_2} \right| \cdot 100 \qquad (1)$$

where $e_{r_{T_2\%}}$ is the relative error expressed in percentage, T_{2_m} is the measured period and T_2 is the input period.

For the analysis of the error performances we propose a test methodology based on functional simulations using VHDL, with the objective of analyzing the error on the output characteristic of the mixer through the simulation of its logical behaviour [10]. This allows us to analyze the error performance regardless of the technological issues and their error contribution, which is important to define an ideal logical model of the system.

To measure the error performance it is essential to introduce a device that reads the informative parameter of the mixed signal (i.e. frequency or time) and converts it into a numerical quantity. This device will be connected to the mixer in a master-slave mode. The mixer and the receiver model the Device-Under-Test (DUT), although in this design we simply aim to fully inspect the functional simulations of the mixer.

Fig. 3 shows the conceptual structure of the test-bench, which provides the input stimuli to the DUT and shows the system response. The test-bench along with the RTL (register transfer level) description of the DUT are implemented in VHDL and simulated with Modelsim, from Mentor Graphics.

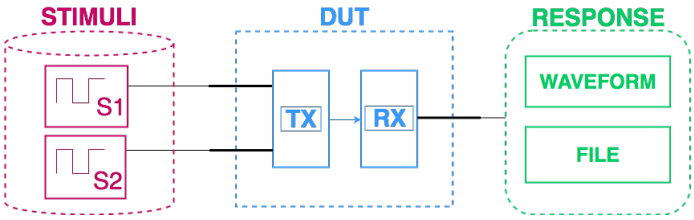

Fig. 3. Conceptual representation of the test-bench used in the functional simulation. The input stimuli are two square-waves, of different frequencies, generated with a specific relative phase shift. The receiver will provide some numerical information related the mixed signal. They are written into a text file, and the results are then processed to retrieve the error information. All the signals involved in the test-bench can be visually inspected through the waveform viewer to check whether the results match the expectations.

The whole system is simulated for different combinations of known values of f_1, f_2 and $\Delta\phi$. The total number of input samples has been fed with a 10x10x10 array. This is in total 1,000 samples. The results stored into the text files are then processed, and the error is evaluated according to Eq. 1.

A. Design of the Receiver Architecture

It is important to ensure accuracy in performing the frequency-to-code conversion for the design of this block as a

significant error contribution to the measurement would make the results inconsistent for characterization. Additionally, it is fundamental to keep the hardware complexity of the receiver low to speed-up the whole simulation process for a simpler debugging process. The complete architecture is shown in Figure 4.

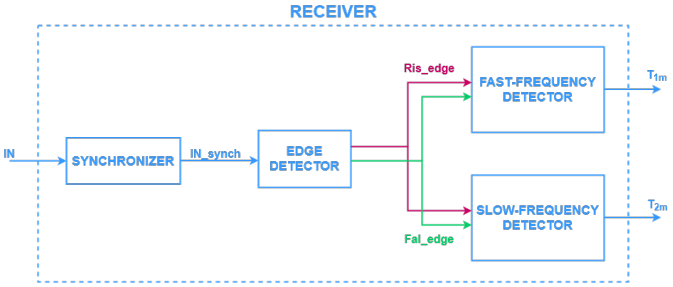

Fig. 4. Top level view of the receiver. This architecture consists of four building blocks: (1) a synchronizer, (2) an edge-detector, (3) a fast-frequency detector, and (4) a slow frequency detecor.

The measurement principle exploited by the receiver is the edge-to-edge time difference to code conversion, which implies the use of a reference clock signal with frequency f_{ck}. The synchronizer brings the external input signal into the timing domain of the system clock, thus providing the synchronous notification of the incoming asynchronous edges. To prevent data from being lost during synchronization, the following equation must be satisfied [11]:

$$\frac{1}{f_{ck}} = T_{ck} < min\{T_{IN}\} \tag{2}$$

where f_{ck} is the clock frequency of the synchronizer and the receiver, and $min\{T_{IN}\}$ is the minimum pulse of the asynchronous input signal. The following edge detector generates two synchronous signals that are active when either a rising or a falling edge is detected. The "Ris_edge" signal enables the fast-frequency detector which is a high-pulse counter, while the "Fal_edge" signal disables the counter which is then synchronously reset to be used for next conversion. This behaviour is similar for the slow-frequency detector, which is instead a low-pulse counter. The use of two dedicated counters allows for a simultaneous measurement of the two periods within the mixed signal.

B. Analysis of the Accuracy of the Receiver

During the synchronization stage, a certain error on the period of the synchronized signal (IN_synch) could arise, as described in Fig. 5.
Assume that $2\ T_{ck} < T_{IN} < 3\ T_{ck}$ and consider four successive rising-edges of the reference clock (CK). The input signal (IN) can have a low-to-high transition some time (Δt_a) after the first edge of CK and a high-to-low some time (Δt_b) before the third edge of CK. The period of the asynchronous input signal can be expressed as:

$$T_{IN} = 3\ T_{ck} - \Delta t_a - \Delta t_b \tag{3}$$

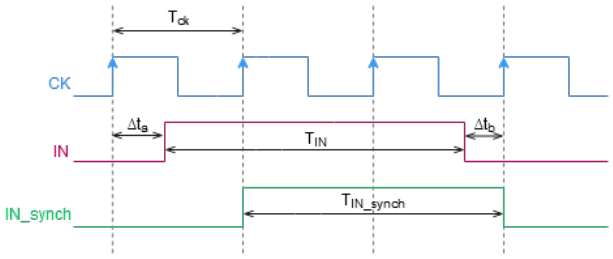

Fig. 5. Timing diagram related to the synchronization stage at the receiver side and the error on the resulting synchronized signal

While the period of the synchronized input signal is:

$$T_{IN_{synch}} = 2\ T_{ck} \tag{4}$$

The absolute error on the input signal after the synchronization can be evaluated as:

$$\epsilon_{T_{IN}} <= \mid 3\ T_{ck} - \Delta t_a - \Delta t_b - 2\ T_{ck} \mid \tag{5}$$

Depending on Δt_a and Δt_b, $\epsilon_{T_{IN}}$ can assume different values:

1) If Δt_a, $\Delta t_b \longrightarrow 0$, $\epsilon_{T_{IN}} \longrightarrow T_{ck}$
2) If Δt_a, $\Delta t_b \longrightarrow T_{ck}$, $\epsilon_{T_{IN}} \longrightarrow \mid -T_{ck} \mid = T_{ck}$
3) If Δt_a + $\Delta t_b \longrightarrow T_{ck}$, $\epsilon_{T_{IN}} \longrightarrow 0$

In conclusion, we can state that the relative percentage error on T_{IN} is:

$$\epsilon_{r_{T_{IN}}}\% <= \frac{T_{ck}}{T_{IN}} \cdot 100 \tag{6}$$

Supposing that an error of 0.1% is acceptable, T_{ck} should be at least three order of magnitude smaller than T_{IN}.

Figure 6 shows the timing diagram with all the steps of the conversion chain, and it refers only to the high-pulse counting process. After the synchronizer, the input signal is synchronous

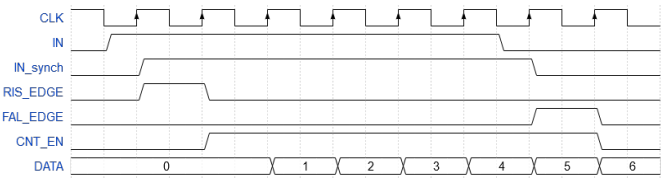

Fig. 6. Example of timing diagram related to the high-pulse counting process at the receiver. IN is the asynchronous input signal. IN_synch represents the synchronous version of the receiver input signal, whose pulse length is the same as the one of the CNT_EN signal, which demonstrates that no further error arise during the edge detection.

with the internal clock. As the following edge-detection and pulse-to-code conversion occur coherently with the clock, no further error is logically generated.

To improve the system accuracy we still need to set two parameters for the design of the two counters:

1) The period of the clock signal (T_{ck}), which fixes the resolution of the counter
2) The number of bits of the counter (N), which is in related to the clock and the input signals, determining the count length.

Suppose we first choose the clock frequency according to the target resolution, then the number of bits of the counter can be set as:

$$N > \log_2 \frac{\Delta t}{T_{ck}} \tag{7}$$

where Δt is the target pulse length in seconds and T_{ck} is the clock period.

III. Simulation results and Analysis of the system error performance

In this section we aim to characterise the trend of the error with respect to the input frequency ratio, including the effect of $\Delta\phi$. The error performed on T_2 is expected to decrease with the increase in the frequency ratio ($\frac{f_1}{f_2}$). In particular, if we assume that the maximum acceptable relative error on T_2 is of the 10%, f_1 should be at least one order of magnitude grater (x10) than f_2 [9]. Additionally, the impact of the phase shift is expected to be significant towards lower frequency ratios.

A. Results

Fig. 7, 8, and 9 provide some general information related to the trend of the error with the input frequency ratio. In each graph you can clearly observe that the overall trend is exponentially decreasing, and when f_1 is three orders of magnitude greater than f_2 (i.e. from the fourth decade of each graph), the error reduces to almost 0%.

The difference among the graphs lies in the way the phase shift is encountered for the evaluation of the error, and it determines the dot distribution in each scatter plot. In particular, Figure 7 shows the trend of the average error on T_2 as a function of the input frequency ratio. Each dot of the scatter plot corresponds to the error evaluated for a specific $\frac{f_1}{f_2}$ and averaged over all the possible $\Delta\phi$ for that specific frequency ratio.

Fig. 8, shows the trend of the maximum error on T_2 as a function of $\frac{f_1}{f_2}$. Specifically, each dot of the scatter plot refers to the maximum error evaluated for a specific input frequency ratio and for a specific phase shift giving that maximum value.

The dot distribution changes towards lower frequency ratios, with respect to the average case shown in Fig 7. In particular, you can clearly observe that the limit error of the 10% previously set is overcome and a maximum value of the 12% is reached, despite the same input frequencies are considered.

Fig. 9 shows the trend of the minimum error on T_2 as a function of $\frac{f_1}{f_2}$, where each dot of the scatter plot refers to the minimum error evaluated for a specific input frequency ratio, arising for a certain phase shift. In this case, the scatter plot shows that for some specific combinations of frequency ratio and phase shift, the error on T_2 assumes the value of 0% even when the f_2 is only one order of magnitude greater than f_1.

In conclusion, the phase shift impacts significantly on the error towards lower input frequency ratios, as well as the values in the second and the third decade in each graph. From the fourth decade on, there are no significant variations between the scatter plots, and the error reduces exponentially to the 0%.

B. Analysis

1) The mathematical equation: The equation that links the error rate to the input frequency ratio is a decaying exponential and it can be written in a parametric form as:

$$e_{r_{T_{2\%}}} = A \cdot e^{(-B \cdot log_{10}(\frac{f_1}{f_2}))} + C \tag{8}$$

where $e_{r_{T_{2\%}}}$ is the relative percentage error on the period T_2, $\frac{f_1}{f_2}$ is the input frequency ratio and A, B and C are the coefficients. From the fitting curve of the average error on T_2 in Fig. 7 we can extract the coefficients, and the equation becomes:

$$e_{r_{T_{2\%}}} = 154.122 \cdot e^{(-2.281 \cdot log_{10}(\frac{f_1}{f_2}))} + 0 \tag{9}$$

2) The effect of the phase shift: Fig. 8 and 9 highlight some details regarding the effect of the phase shift for specific frequency ratios in the red boxes. To analyze it in greater detail, we can study the output characteristics of the mixer.

Fig. 10 and 11 demonstrate the effect of the phase shift on the error generated on T_2 in the mixed signal. They show two timing-diagrams of the signal mixing, where the input frequency ratio is the same and in equal to 25 while the relative phase shift is different.

In particular for Fig. 10 when $\Delta\phi$ is at 0%, no error is generated as T_{2_m} equals T_2. Conversely, in Fig. 11 when $\Delta\phi$ is equal to 50% a significant error arises, since the last high pulse in MIXED_S present in Fig.10 disappears in this case precisely because of the phase shift. The error can be evaluated as follows:

$$T_2 = 12.5 \cdot T_1$$

$$T_{2_m} = 11 \cdot T_1$$

$$e_{r_{T_2\%}} = \left| \frac{T_2 - T_{2_m}}{T_2} \right| \cdot 100 = \left| \frac{12.5T_1 - 11T_1}{12.5T_1} \right| \cdot 100 = 12\% \tag{10}$$

IV. Trade-off between power consumption and error performance in digital mixing

Increasing the frequency ratio represents a safe solution to improve the error performance in digital mixing. However, this has a trade-off on the power consumption of the system. Hence, it is essential to estimate the cost in terms of power of a specific input frequency ratio to determine the trade-off between error performance and power consumption for a certain application.

The characterization of the system power consumption implies the definition of a model that takes into account the circuit implementation details. In this analysis we will consider CMOS technology for the implementation.

The sources of energy consumption on a CMOS chip can be classified in general as static and dynamic power dissipation, and the main difference between them is that the latter is frequency dependent, which is a key variable for this analysis.

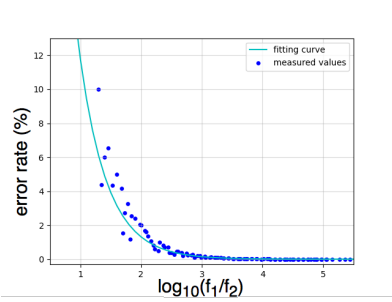

Fig. 7. Average error on T_2, showcasing the error from the results collected in the simulations averaged over different $\Delta\phi$ for each $\frac{f_1}{f_2}$. The fitting curve shows the general trend.

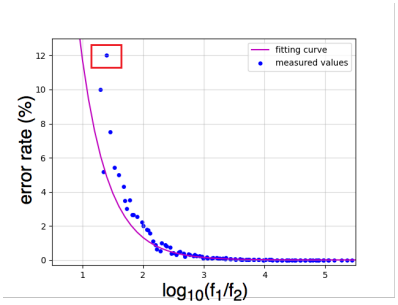

Fig. 8. Maximum error on T_2, showcasing the maximum error from the results collected in the simulations for specific $\Delta\phi$ and $\frac{f_1}{f_2}$. The section in red shows that the error overcomes the limit of the 10%.

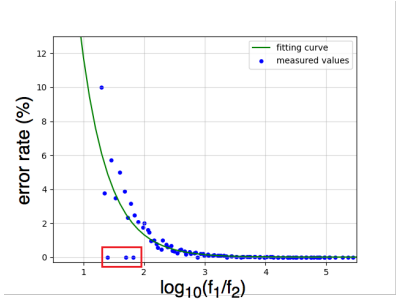

Fig. 9. Minimum error on T_2, showcasing the maximum error from the results collected in the simulations for specific $\Delta\phi$ and $\frac{f_1}{f_2}$. The section in red shows that the error due to may reach the 0% even for sufficiently small frequency ratios.

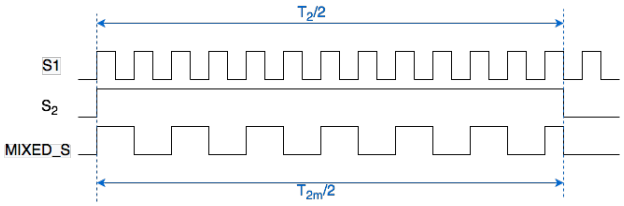

Fig. 10. Example of timing diagram of digital mixing. T_2 is the period of the input signal S_2, while T_{2_m} is the period of S_2 in the mixed signal. No error on T_2 is generated in the mixed signal. The relative phase shift among S_1 and S_2 is of the 0%, and the frequency ratio is equal to 25.

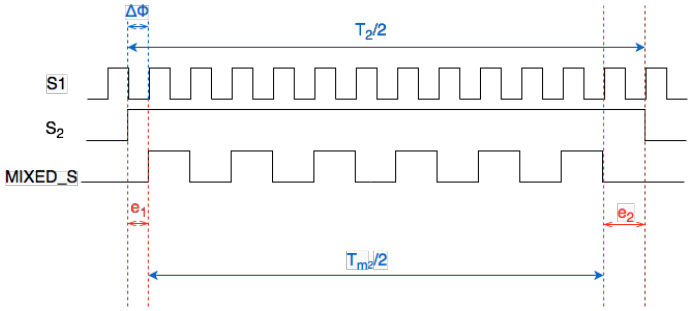

Fig. 11. Example of timing diagram of digital mixing. The error on T_2 generated in the mixed signal is equal to the 12%. The relative phase shift among S_1 and S_2 is of the 50%, and the frequency ratio is equal to 25.

In a first order approximation, the dynamic power consumed by a CMOS circuit can be estimated according to the following formula:

$$P_{dyn} = C_{eff} V^2 f \tag{11}$$

where P_d is the power in Watts, C_{eff} is the effective switch capacitance in Farads, V is the supply voltage in Volts, and f is the frequency of operations in Hertz [12].

According to Eq. 11, the dynamic power is linearly dependent on the clock frequency, which corresponds to f_1 for the mixer. For the case of f_2 which represents the frequency of the reset signal, no significant variations on the dynamic power are expected as its frequency varies. This is expected since it determines the time intervals in which the circuit is ON and OFF. The dynamic power in this case would be reduced only if the duty cycle of the reset is reduced as well. Therefore, the expected trend of the total power consumed in the D flip-flop as a function of the input frequency ratio is linear. It can be represented by a straight line not passing through the origin since the total power consumed is also a function of the leakage power, which is constant with the frequency of the input signals. Moreover, the slope of this straight line will be determined by the product $C_{eff}V^2$, which is dependent on the target technology for the implementation.

A. Analysis of the Dynamic Power in digital mixing and study of the error-power trade-off.

The method we propose for this analysis is based on the RTL synthesis of the D flip-flop mixer with the aid of *Synopsys*, in order to verify the actual trend of the power consumed as a function of the input frequency ratio. The results obtained from the synthesis of the mixer are shown in Fig. 12. The straight lines refer to the dynamic power consumed in the mixer as a function of the input frequency ratio for different f_2, while the decaying exponential curve represents the fitting curve of the average error on T_2, as shown in Fig. 7. The linear trend of the dynamic power follows our expectations. Additionally, you can observe that as f_2 increases, each curve is progressively shifted upwards. This behaviour is a result of the way the reset signal is created by the synthesizer along with the time interval the compiler considers for the estimation of the dynamic power. If the reset starts and stops with a 0 logic value, the dynamic power estimation starts and stops with the ON state of the mixer. This means that the synthesizer computes the dynamic power considering an odd number of ON states, and an even number of OFF ones. As a result the dynamic power increases with f_2. The specific amount of increment will depend on the total number of periods (integer or fractional) of the reset signal considered by the compiler to compute the dynamic power.

The optimum operating condition of the mixer is defined by the intersection points resulting from the combination of the plots. In particular, they represent points of global minima that define the best power versus error trade-off in digital

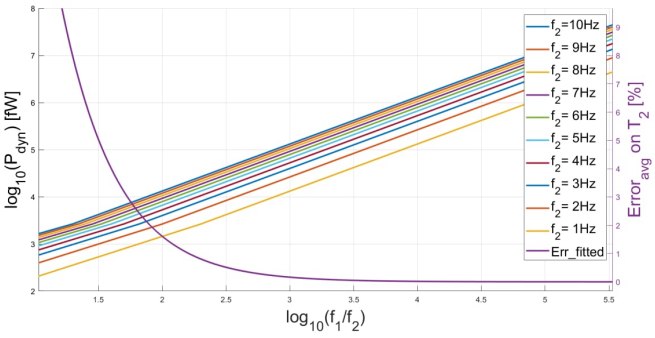

Fig. 12. Combined (1) error and (2) power plots. (1) is the fitting curve of the average error on T_2 red

as shown in Fig. 7. (2) is a set of straight lines for different f_2 representing the dynamic power consumed in the mixer as a function of $\frac{f_1}{f_2}$.

mixing in terms of input frequency ratio. This trade-off can be achieved with a careful design of the input frequency levels for a specific target application. Such points belongs to the following interval:

$$1.5 < log_{10}\left(\frac{f_1}{f_2}\right) < 2$$

V. Conclusion and Future Work

This paper investigates the feasibility of a low power communication protocol based on a multiple input, single output data transmission method, which employs a D flip-flop as a digital mixer. In particular, this research focuses on the characterization of the system in terms of error and power metrics. We have demonstrated with a test methodology based on functional simulations that the main sources of error are the frequency ratio of the reset and clock signals and their relative phase shits, and we have shown that the error performed on the lower frequency information as a function of the frequency ratio has a trend which is exponentially decreasing. Additionally, we have proved that the phase shift may impact the system error performances towards lower frequency ratios. Moreover, with the power analysis we have demonstrated dynamic power consumed by the mixer is linearly dependent on the clock frequency, under the assumption that the circuit implementation is based on CMOS technology. Finally, we have investigated the best power versus error trade-off in terms of input frequency ratio. Future work would involve the study of the possible issues arising from the actual circuit implementation on a specific technology. This implies the study of additional details such as the effect of the phase jitter associated to the clock and the problem metastability. Additionally, a more accurate estimation of the power consumption at the circuit and RTL levels can be achieved. Moreover, the effect of the reduction of the duty cycle of the reset signal in the power consumption will be investigate, with the objective of increasing the spectrum of solutions for the design of the frequency levels of the input signals.

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