Design of an Active Rectifier for Wireless Power Transmission Systems

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Abstract

Implantable Medical Devices (IMD) are being used in the form of cochlear implants, pacemakers and neural implants to monitor, sense and stimulate various processes. These devices might have batteries which have limited lifetime and capacity, and are very bulky. Moreover, they pose health and safety concerns, since surgery might be required to replace these batteries and cause the risk of complications. The solution to this is to either reduce the size of the battery or to completely remove the need for a battery by supplying power to the implant with the help of Wireless Power Transfer (WPT) techniques. The power that is harvested by the implant needs to be converted from AC to DC to supply power to the rest of the chip. This is achieved with the help of rectifiers. However, many important factors need to be considered while designing these rectifiers. They need to have a high Power Conversion Efficiency, since the power harvested by the inductive link is already very low. The size of these rectifiers also needs to be taken into consideration, as the goal while designing IMDs is to make them as small as possible. This thesis presents the research done on WPT techniques, Active Rectifiers and its issues and compensation techniques. The circuits are designed in TSMC 180nm technology using Cadence tools. The simulations are done in Spectre and then exported to MATLAB to be plotted into figures. The system simulations are done for a frequency of 433MHz, and achieved a PCE of 56.9% with an output power of 9mW. The achieved VCR was 79.5% with a 2V output voltage with a 500 ohm load and is used to supply a Bandgap Reference and Low-Dropout Regulator circuit.

Acknowledgements

I would like to thank my supervisor Dr. Pantelis Georgiou for all the encouragement, guidance and support during the phase of this project. He also helped me to take control of my project and offered me a good choice of topics to research and design on.

I would also like to thank my mentor Mr. Daryl Ma for our discussions on the implementation of Active Rectifiers in Implantable Medical Devices and also for helping me solve various problems that arose while designing these devices.

Last but not least, I would like to thank my parents and friends for their continuous support and motivation throughout the duration of my Masters course.

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Abbreviations

AC: Alternating Current

AR: Active Rectifier

CM: Current Mode

DC: Direct Current

IMD: Implantable Medical Devices

IPT: Inductive Power Transfer

ISM: Industrial, Scientific and Medical

IC: Integrated Circuits

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

PCE: Power Conversion Efficiency

RFID: Radio Frequency Identification

TG: Transmission Gates

UHF: Ultra High Frequency

VCR: Voltage Conversion Ratio

VM: Voltage Mode

WPT: Wireless Power Transfer

ZVS: Zero Voltage Switching

Chapter 1

Introduction

1.1 Motivation

IN recent years, there has been an increase in the applications of Implantable Medical Devices (IMD).From cochlear implants, to pacemakers and neural implants, IMDs are being used to monitor, detect and stimulate various physiological processes. The goal while designing these devices is to minimize the size of the devices, and make them less invasive and to increase their lifetime, and have good reliability after being implanted into the human body. The technology development in minimizing the size of the electronic components has been extremely successful due to CMOS processes (reaching the 5nm technology size). However, the technology to power up these IMDs with the help of energy storage elements has been slow to follow.

In recent devices, the battery is the element that takes up the bulk of the implant. These energy storage elements also have a finite capacity and limited lifetime. Replacing these batteries require surgery and increase the chances of complications. There also is a risk of the battery rupturing during surgery or while being implanted in the body which can cause serious health and safety concerns.

The solution to the energy storage issue is to use Wireless Power Transfer (WPT) techniques. With the help of WPT, there are two routes that can be taken. Either the size of the battery can be reduced, since it can be recharged or can be used to supplement

the harvested energy, or the battery can be completely removed, and the IMD can be used only when the power supply is present. There are many WPT techniques but the most common one is using electromagnetic waves and Inductive Power Transfer (IPT), which involves the use of two coils. On the implanted side, the received AC voltage needs to be rectified and converted to a DC voltage before it can be used to power up the load circuits. The PCE and VCR are therefore important characteristics which determine the quality of the rectifier. An Active Rectifier (AR) can lead to increased PCE and VCR. It however has some drawbacks to which there exist compensation techniques. Increasing the system operating frequency of WPT systems can help reduce the size and cost associated with manufacturing such devices.

1.2 Objectives

The objectives of this thesis is given below:

- To research the need for Wireless Power Transfer and the different WPT techniques
- To understand the working of an Active Rectifier, its issues, and compensation techniques.
- To design an Active Rectifier to be used in a 433MHz system, and simulate it with a pre-designed Bandgap Reference, and Low-Dropout Regulator.

1.3 Thesis Outline

Chapter 2 contains a detailed review on Wireless Power Transfer as well as the different WPT techniques. It also contains a review of on-chip rectifiers, active rectifiers, the issues with active rectifiers and finally the compensation techniques that exist to increase the PCE of the active rectifiers.

Chapter 3 includes the implementation and simulation of the lower frequency active rectifiers which are taken from the past research. An attempt was made to use the compensation techniques in a higher frequency system, and the design choices made are also given

in this chapter.

Chapter 4 gives a conclusion of the work presented in this thesis. Finally, the design choices and the limitations and challenges of designing high frequency systems are discussed.

Chapter 2

Literature Review

2.1 Introduction

THIS chapter contains a detailed review on existing Wireless Power Transfer techniques, On-chip rectifiers, and compensation techniques

2.2 Wireless Power Transfer

Wireless Power Transfer is the transfer of electrical energy without a physical link. In WPT, there are many established techniques to transfer power, with electromagnetic WPT being the most emerging one. Infrared and Optical methods pose various challenges and can be unreliable during severe weather conditions. Nikola Tesla was an important figure in the development of WPT. He was able to successfully power up a lamp with the help of coils in 1981, and later performed experiments to transfer power over longer distances. In the past two decades, the application of WPT has been growing in IMDs, RFID, wireless charging and powering up of electronic devices due to development in low powered ICs and the market need for more battery-less applications. Significant development in the field of WPT can revolutionize many sectors ranging from Information Technology sector to the Biomedical Engineering sector [3].

Previously, the transmission of power was done using trans-cutaneous cables, and

involved the use of batteries. In applications involving the use of batteries, the limited lifetime of the battery, and the finite amount of charge that can be stored poses substantial challenges. Replacing the batteries also requires surgery and can increase the risk of complications [4].

WPT can be broken down into two distinct categories: Near-field WPT and Far-field WPT. For any application to be classified at near-field, two conditions should be met: Firstly, the distance between the two coils should be less than one wavelength (λ) at the system frequency. For a frequency of 433MHz, the wavelength is 69.24cm considering air as the medium. Secondly, the largest diameter of the primary source coil should be less than ($\lambda/2$). Using the Ultra High Frequency (UHF) ISM bands which is between 300MHz to 3GHz as the system frequency can lead to a smaller size and lower cost solution. There are different ways to transfer power in near-field WPT, namely inductive coupling and resonant coupling [1].

2.2.1 Inductive Power Transfer

In IPT, there are two coils, namely the 'primary' and 'secondary' coils. In IMDs, the primary coil is the external source, and the secondary coil is implanted, and provides power to the chip. The distance between the two coils and the alignment of the coils heavily influence the efficiency the system can achieve. The earliest reported use of IPT was in the 1960s, which used a primary coil on the surface of the chest, and a similar coil within the chest [5]. In IMDs, the medium between the two coils is several layers of skin. A biomedical system is shown in Fig. 2.1. The system consists of two sides, the primary and secondary side. The primary side is the one that supplies energy to the secondary side and consists of a DC source, a DC-AC converter to achieve the system operating frequency, and then a tuning circuit to transfer power or data through a coil. The secondary side is the implanted side. It consists of a coil, tuning circuit, an AC-DC converter (rectifier) and finally a DC-DC regulator to either power up a load or to charge a battery.

The goal while designing devices that use WPT is to achieve high efficiency, but there are many challenges that are faced. Firstly, since the secondary side is implanted,

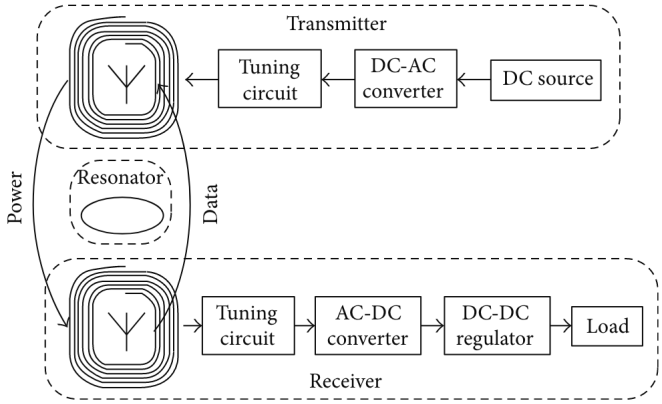
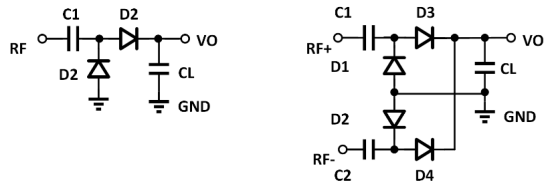


Figure 2.1: Model of a WPT System [1]

there are restrictions on the coil size and a smaller coil results in a lower coupling coefficient and lower efficiency. Secondly, an increase in the system frequency will increase efficiency, but the trade-off is a higher energy loss through the skin, which will cause heating issues and safety concerns. The next challenge is the alignment of the two coils. The alignment of the primary coil can easily be controlled, but the secondary coil is implanted in some cases and there is no control on it after the surgery has been completed. Hence, it poses a significant challenge. The angular and lateral misalignment of the coils can cause the efficiency to decrease. Another challenge for the lower power applications is the level of output power that is required, since the efficiency is proportional to power level. Modelling these systems are also challenging as the medium between the two coils must be known. Optimization to the primary coil can be done while considering a couple of factors, such as the distance between the two coils are fixed, or in cases where the secondary coil is not fixed (capsule endoscopy), a general predicted range can be taken and optimizations can be done [1].

2.3 On-chip Rectifiers

A fundamental component of the receiver side is the AC-DC converter (also known as a Rectifier), which is used to power up the load circuits. The important factors to consider while designing rectifiers is the Power Conversion Efficiency (PCE) and the Voltage



(a) Single-ended (b) Differential

Figure 2.2: Schematics of (a) Single-ended and (b) Differential Rectifier [2]

Conversion Ratio (VCR). There are two categories in which rectifiers can be placed: single-ended or differential as shown in the Fig. 2.2. They can also be split into half-wave and full-wave rectifiers depending on whether they conduct during half a cycle or over the entire cycle.

Karthaus et al. designed a passive UHF RFID transponder with a rectifier circuit which used specially designed Schottky diodes with a low turn-on voltage, low resistance and high saturation current [6].Designing special devices however increases the fabrication costs as it leads to an increase in the number of masks required, and makes it impractical for a low-cost design.

Yi et al. proposed the use of MOS transistors with very low threshold voltage in a multi-stage architecture. Using multiple stages would seem to reduce efficiency, but it was shown that a multiple stage rectifier with specified output power was able to maintain the maximum achievable efficiency and would not cause a decrease in efficiency despite the increase in the number of stages [7]. Another issue encountered is that low threshold voltage transistors had lower transconductance which led to a lower performance compared to that of a diode [8].

Umeda et al. proposed a threshold voltage compensation technique which involved first charging a secondary battery present in the receiver side and then distributing that voltage between the gate-drain terminals and was able to achieve a PCE of 1.2% [9]. The disadvantage of using this compensation technique is the requirement of a secondary battery on the implanted side which goes against our goal of designing a battery-less application.

Kotani et al. proposed the use of a multi-stage cross-connected rectifier in a differential configuration in 180nm CMOS technology. The problem with this proposed architecture is the reverse leakage current that occurs with high input levels [10].

2.4 Active Rectifiers

Ghovanloo et al. compared various full-wave rectifier topologies to reduce the substrate leakage current and other parasitic components to improve the systems high frequency operation. One of the designs included replacing the top two passive diodes with PMOS switches, and the bottom two passive diodes with diode-connected NMOS switches in order to reduce the reverse current. The efficiency of the system was however not fully optimized [11].

Lam et al. proposed an active rectifier system which replaced the Schottky diodes with cross-coupled PMOS switches and comparator controlled NMOS switches and compared the operation of the two schemes. The proposed design had a turn-on delay of 2ns which can be tolerated for lower frequencies, but struggles at higher frequencies. The VCR of the proposed rectifier significantly dropped after a operating frequency of 20MHz [12].

The comparator compares the drain to source voltage of the NMOS devices and goes high when the supply voltage is negative and allows the NMOS to switch on and conduct. The use of comparator however adds a time delay to the circuit. In order to reduce the size and power consumption of the comparator, a gate driver circuit is further required to drive the NMOS switches during the negative cycle. This gate driver element adds another time delay to the circuit. The two delays cause a turn-on delay which reduces the VCR by lowering the conduction time, and a turn-off delay which lowers the PCE due to a reverse current flow in the NMOS switches during the positive cycle of the supply voltage. These delays due to the comparator and gate driver cells can be reduced by causing the comparator to adaptively trip earlier by adding an offset voltage. [13].

There are two different methods to add an offset voltage to the comparator. The first method directly adds a voltage to the input of the comparator and is known as Voltage

Mode (VM) compensation. It benefits in lower power consumption since the voltage is added without drawing extra current from the supply, but has limited compensation range and accuracy. The second method is achieved by injecting a current into the comparator arms which causes an offset voltage to be added to the comparator circuit, and is known as Current Mode (CM) compensation. The benefit of using CM is a larger compensation range. The trade-off is a higher power consumption since it needs to draw extra current from the supply. Another drawback is that the injected currents need to be switched fast for either the on or off compensation, which causes it to be impractical to be used at frequencies higher than 13.56MHz [14].

Chapter 3

Design

3.1 Introduction

IN this chapter, the initial design and simulations are done for a system frequency of 13.56MHz using the active rectifier designed by Cheng et al [14]. A series of design changes are then made in an attempt to use the active rectifier in a 433MHz system as per the required specifications. This however was not possible due to various issues which are also highlighted in this Chapter.

The time period of a signal at 13.56MHz is 73.746ns, and the conduction time of the NMOS power switches are between 20ns to 30ns. All the relevant circuit diagrams are in the Appendix A. An important metric to evaluate active rectifiers is the Power Conversion Efficiency (PCE) and Voltage Conversion Ratio (VCR).

The PCE of a Rectifier is given by:

$$\begin{aligned} PCE &= \frac{P_{out}}{P_{in}} \\ P_{out} &= V_{DD}^2/R_L \\ P_{in} &= \frac{1}{NT}\int_{t0}^{t0+NT} V(t)I(t)dt \end{aligned} \tag{3.1}$$

where T is the time period of the input signal, and N is the number of cycles used while integrating for P_{in}.

The VCR of a Rectifier is given by:

$$VCR = \frac{Vout}{V_{in-peak}} \tag{3.2}$$

where $V_{in-peak}$ is the peak input signal amplitude and Vout is the output voltage of the rectifier.

3.2 Lower Frequency Design

This section of the chapter involves designing and the working of an Active Rectifier designed previously at a 13.56MHz frequency. The learnings from this will then be used to modify the comparator and active rectifier design in an attempt to make it work for the higher frequency specification of 433MHz.

3.2.1 Cross-coupled Rectifier

The first important component in the AR is the cross-coupled PMOS and NMOS devices as shown in Fig. 3.1. V_{AC1} and V_{AC2} are the sinusoidal differential inputs. The gates of the PMOS and NMOS are connected together (M0 and M2, M1 and M3). Depending on the positive or negative part of the cycle, either M0-M3 conduct or M1-M2 conduct respectively. A common modification to this architecture is to keep the cross-coupled PMOS devices and to drive the gates of M2 and M3 with a comparator. The comparator compares the drain-source voltage of the NMOS devices as shown in Fig. 3.2. A gate driver is also used to be able to drive the larger NMOS gates and reduce the driving capability of the comparator, which leads to lower power consumption of the comparator.

3.2.2 Comparator Design

The next important component in the AR design is the comparator. The comparator chosen for these simulations is a common-gate push-pull comparator as shown in Fig. 3.3. The comparator triggers on the negative cycle of the input sinusoidal signal. This comparator adds a certain delay to the circuit.

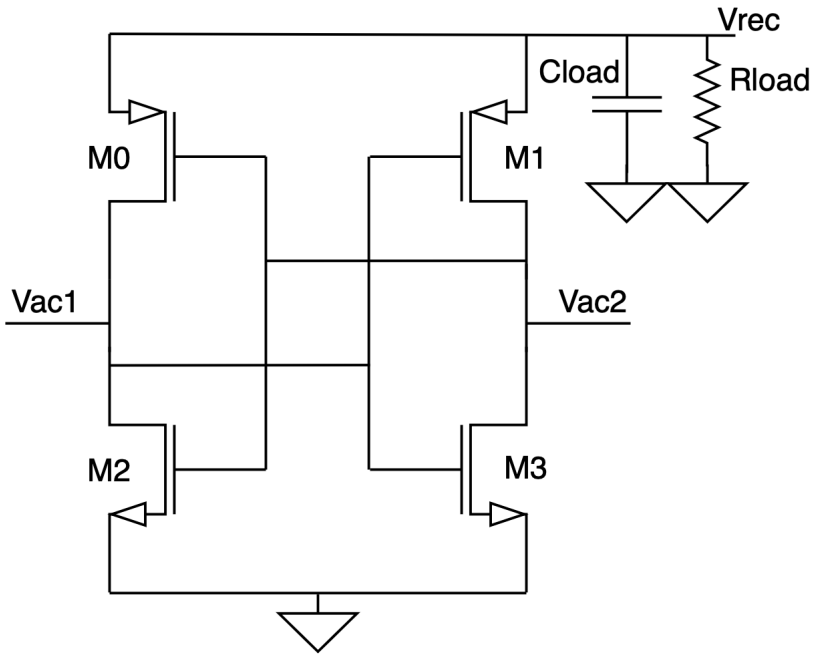


Figure 3.1: Cross-coupled PMOS and NMOS Rectifier

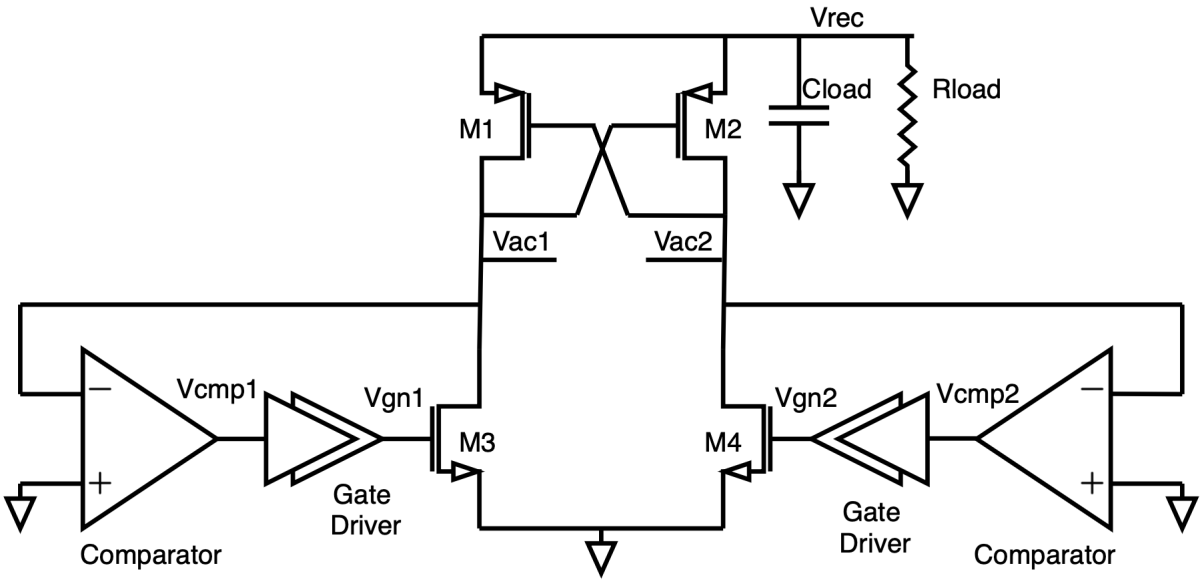


Figure 3.2: Cross-coupled PMOS with comparator controlled NMOS devices

3.2.3 Gate Driver Cells

The next component is the gate driver cells. Since the NMOS devices of the rectifier are of a significant size in order to be able to supply power to the circuit, they are large and

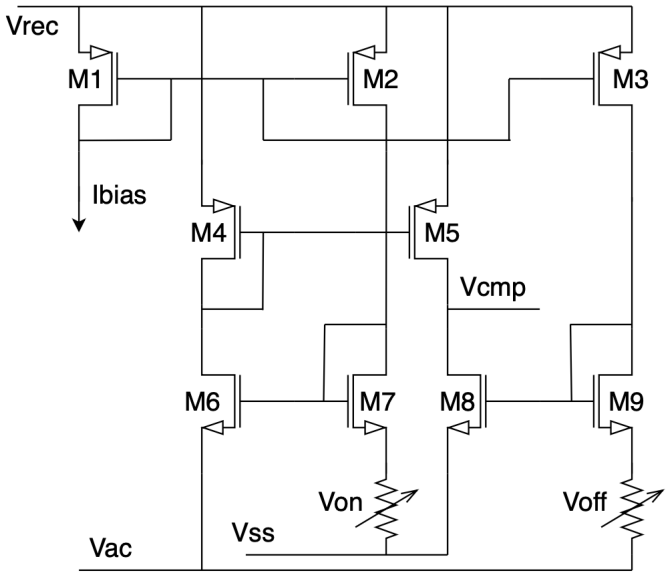


Figure 3.3: Common-gate push-pull comparator

have a specific gate capacitance associated with it. Therefore, after the comparator stage, a set of gate driver cells are used in order to be able to charge the capacitive gate nodes. These are made of simple inverters cascaded together. These gate driver cells also add a delay to the circuit.

3.2.4 VM Compensation

After putting the entire rectifier together as shown in Fig. 3.2. The comparator compares the drain-source voltage of M3 and M4 and outputs a voltage V_{cmp1} and V_{cmp2}. These voltages are then fed to a gate driver cell, and outputs the voltages V_{gn1} and V_{gn2} which are used to drive the NMOS switches M3 and M4 of the rectifier respectively. There are two sources of delay in the circuit, they are from the comparator and the gate driver cells, and this is shown in Fig. 3.4. t_1 is where the comparator is expected to go high, but due to the on-delay, it goes high at t_2. t_3 is where the comparator is expected to go low, but due to the off-delay, it goes low at t_4. These delays cause the comparator to trip later which causes two issues as shown in Fig. 3.5 . Firstly, there is a turn-on delay which reduces the conduction time of the NMOS devices. This affects the VCR of the rectifier. Secondly,

there is a turn-off delay which causes a reverse current through the NMOS devices. This affects the PCE of the rectifier as discussed in the previous chapter.

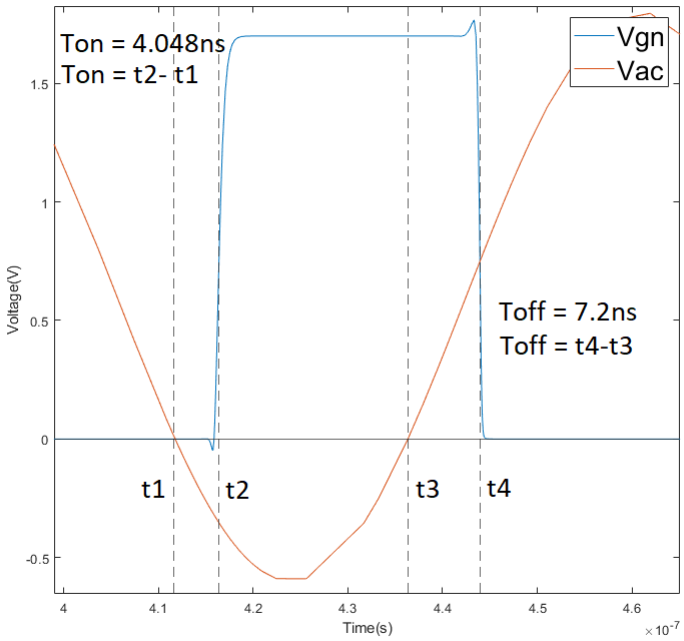


Figure 3.4: Comparator and gate driver delay

There are two common methods to reduce or completely remove these delays as discussed in the previous chapter. The first is Current Mode compensation, which involves injecting an offset current into the comparator arms. This has the effect of charging or discharging the output node. CM compensation has a larger compensation range, but requires fast switching and higher power consumption. The second is Voltage Mode compensation which is the method that is being used in this report. VM compensation adds an offset voltage (V_{on} and V_{off}) with the help of resistors as shown in Fig. 3.3. VM has lower compensation range and accuracy, but works without drawing extra current from the supply. The reason for the lower compensation range, and hence lower resistance values is to keep the devices in saturation region in order to be useful as a comparator circuit.

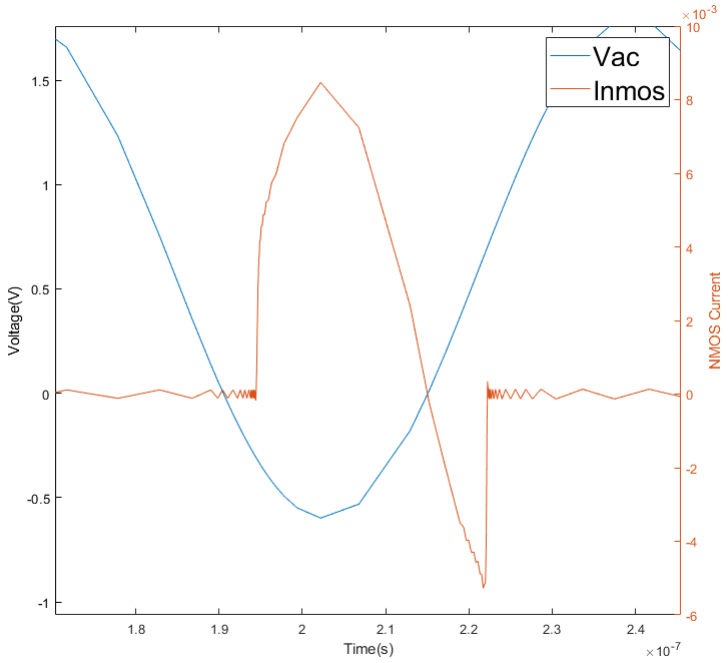


Figure 3.5: Current through the NMOS device

On Delay Elimination

Using the VM compensation, the value of the resistor can be changed to achieve Zero Voltage Switching (ZVS). Firstly, the goal is to achieve ZVS to eliminate the on-delay. On running a parametric analysis using different values of the resistor as shown in the Fig. 3.6, it can be noted how the comparator trips earlier on increasing the value of the resistor ($R1 < R2 < R3 < R4 < R5$) until it completely eliminates the on-delay, or reaches the limit of the compensation range. Another interesting point to note here is that the change in resistor values affects off-delay as well. A solution to this would be to somehow get rid of the offset added by the resistor. This can be achieved by simply adding an NMOS switch in parallel with the resistor. For on-delay elimination, the offset voltage is only required when V_{gn} is low, and therefore, the NMOS is triggered when V_{gn} is high. The achieved output is shown in the Fig. 3.7 and Fig. 3.8, and it can be noted how V_{os} drops to a low value to ensure that comparator works as expected for the off-delay elimination.

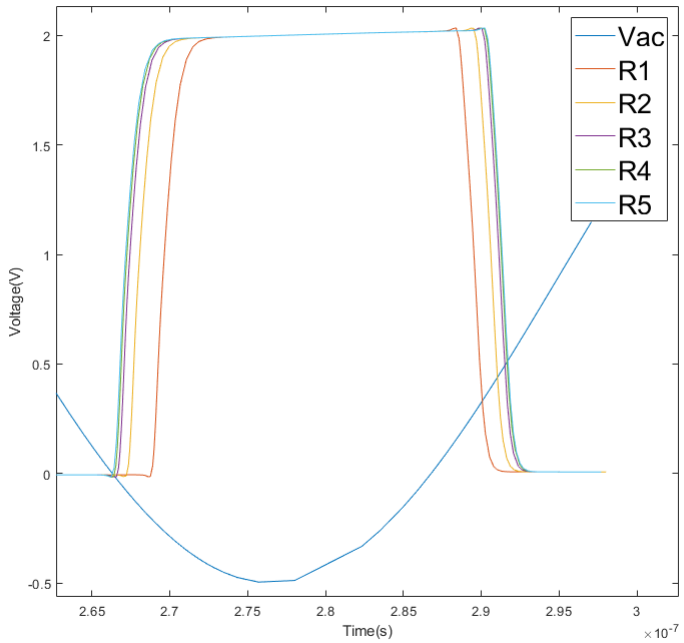


Figure 3.6: On Delay Compensation - Parametric Analysis

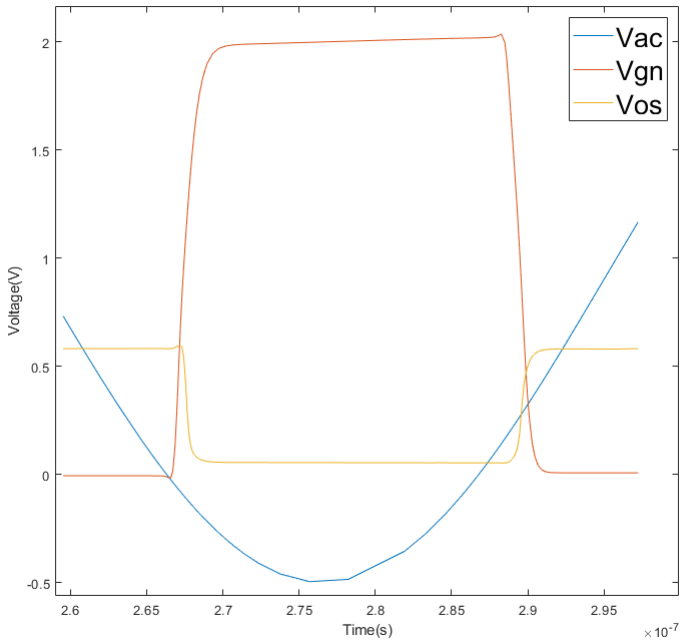


Figure 3.7: On Delay Compensation - Removing offset voltage

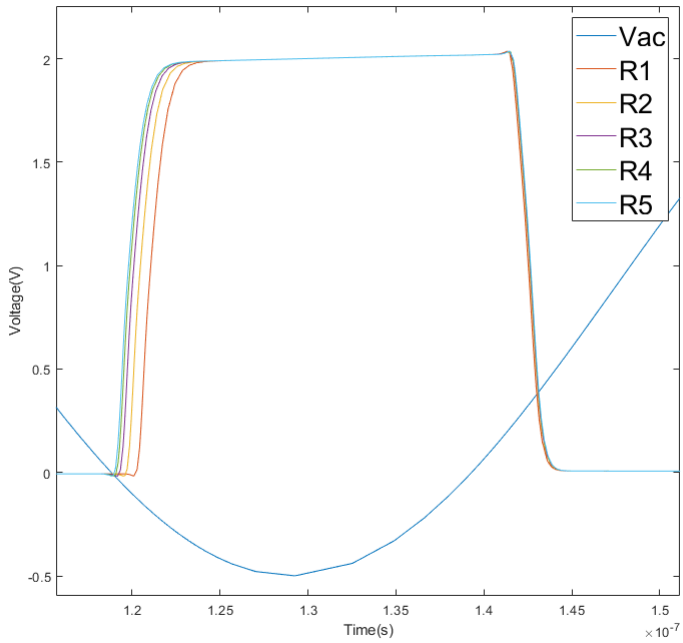


Figure 3.8: On Delay Compensation - Parametric Analysis with offset switching

Off Delay Elimination

Similar to the on-delay elimination, the same steps are repeated for the off-delay elimination. As shown in the Fig. 3.9 , the off-delay reduces with an increase in the resistor value until it eliminates the off-delay. The same method of switching the offset voltage is used here. For off-delay elimination, the offset voltage is needed only when V_{gn} goes high, which would mean that the NMOS in parallel with the resistance needs to be triggered when V_{gn} is low. To achieve this, an inverter is used that takes in V_{gn} and drives the NMOS with the inverted signal.

On/Off Delay Elimination

It is possible to use both on and off delay elimination methods to achieve ZVS and eliminate both on and off delay together as shown in Fig. 3.10. Using the same switching techniques as before, the mode can be changed from on-delay elimination to off-delay elimination depending on the value of V_{gn}.

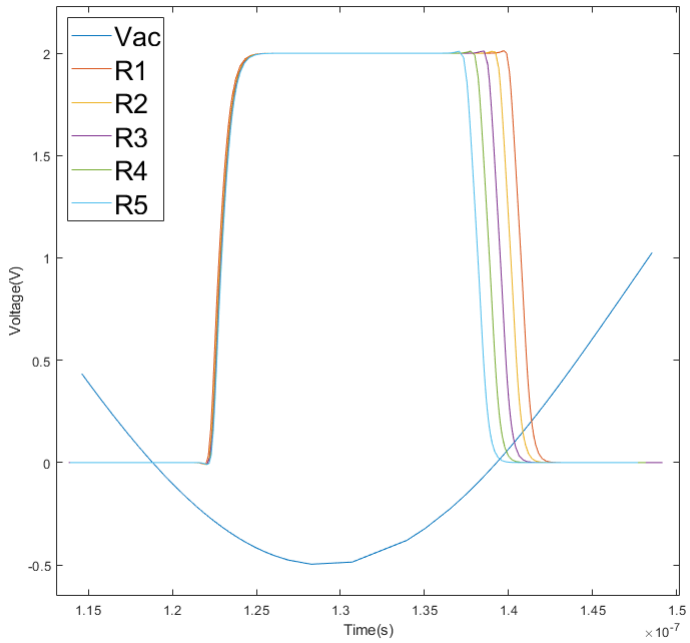


Figure 3.9: Off Delay Compensation - Parametric Analysis

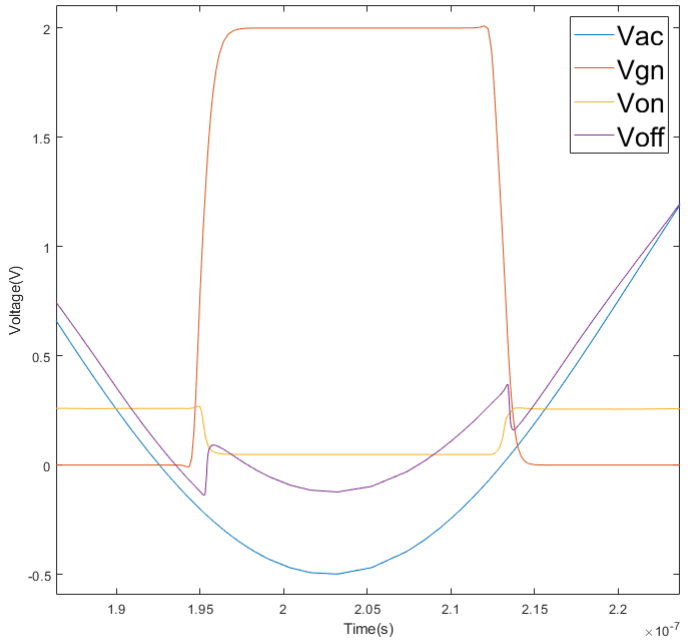


Figure 3.10: On and Off delay compensation

An issue that is encountered when using VM switching is the multiple pulsing issue. Since the on and off offset voltage is being added and removed to the circuit, the reference point that the comparator uses to compare is also being switched. If the two offset voltages overlap due to being high, it can cause the comparator to trip more than once during a negative cycle. This is shown in the Fig. 3.11 and it can be noted that V_{gn} triggers more than once. Many solutions to this problem have been given in Literature. One way of solving this issue is to let V_{gn} trigger, and then have a fixed delay after that before V_{gn} can be triggered again, this way it will only trigger once per negative cycle.

Another solution that seemed to fix the same issue of multiple pulsing is just to have a delay associated with the switching as shown in Fig. 3.12. The previous design removed the V_{on} and added the V_{off} offset voltages at approximately the same instant, and that is believed to have caused the multiple pulsing. By adding a delay so that V_{on} is first removed, and then V_{off} is added to the comparator fixes the problem in the few cases that were tested. This solution however would only work when the conduction time is large. When the system frequency is increased, this solution might cause other problems and fail to work as designed.

The resistors used in this design would ideally be replaced with an NMOS and controlled by the gate of the NMOS to add a variable resistance and offset voltage to the circuit. This allows it to also have a feedback loop, which can dynamically vary the offset depending on the loading conditions of the rectifier as well as the input levels. This however is out of the scope of this report. The current design adds a fixed V_{on} and V_{off} offset voltage and will fail to achieve ZVS under different loading and input power conditions.

The comparator is operated with a 2V supply, 8uA bias current and the power consumption is 268uW for both the comparator and the gate driver cells.

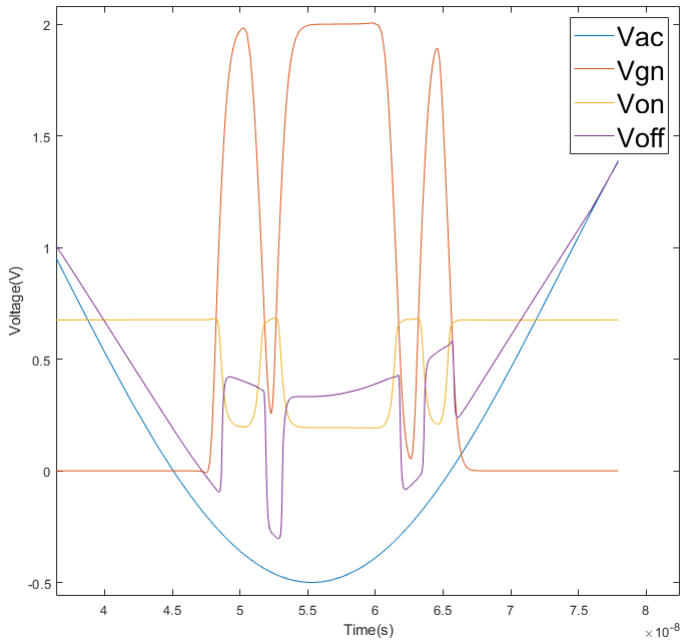


Figure 3.11: Multiple Pulsing issue of the comparator

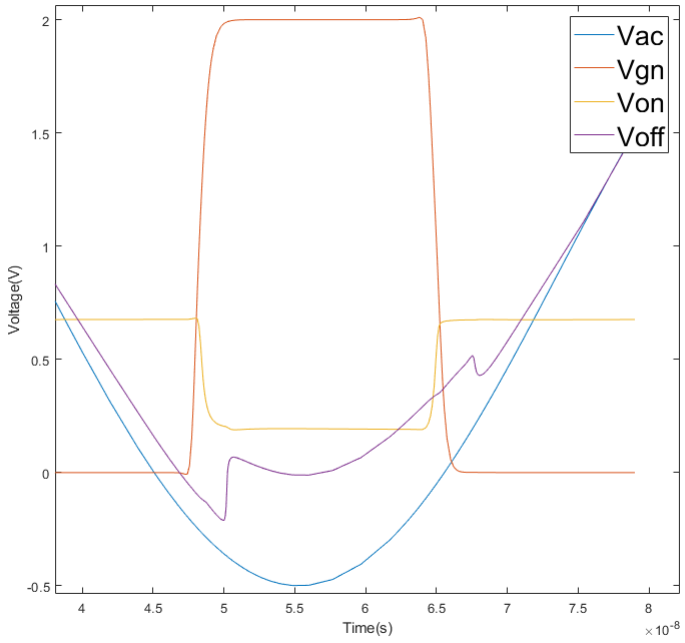


Figure 3.12: Multiple Pulsing - Added Switching Delay

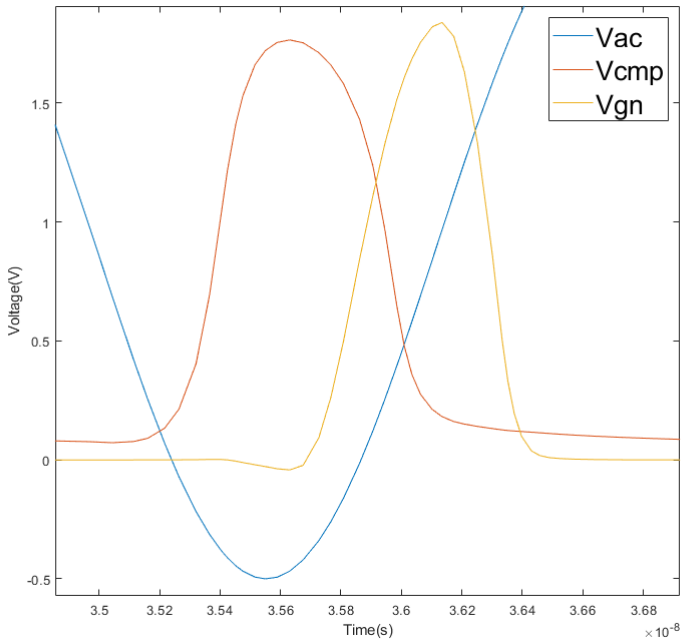


Figure 3.13: VM compensation

3.3 Higher Frequency Design

This section is designed and simulated for a system frequency specification of 433MHz. There are several issues when dealing with high frequencies. The time period of a 443MHz signal is 2.257ns, and the conduction time varies between 0.3ns to 0.9ns. This extremely short conduction time makes it challenging to design a low powered comparator.

3.3.1 VM Compensation

Using the same design techniques from the previous section, a series of design changes are implemented to use the comparator in the higher frequency specification.

The comparator and gate driver cells are powered with a 2V supply, and the power consumption is 7mW. The massive amount of power is consumed by the gate driver cells in order to drive the large gate capacitance of the driver NMOS of the AR. Even though the power consumption is pretty high, there is still significant delay between V_{cmp} and V_{gn} when compared to the zero crossing point of V_{ac} as shown in Fig. 3.13.

The main delay node is the gate driver cells, with the delay being 0.6ns after the zero crossing point. The gate driver cells were required to be able to drive a larger power NMOS so that the comparator sizes could be relatively smaller. The next design will try to bypass the gate driver cells since it adds significant delay to the circuit.

3.3.2 Transmission gates

The next design change attempted was to bypass the gate driver cells with the help of Transmission Gates (TG). There are two TG, one to charge up the power NMOS node capacitance, and one to discharge the power NMOS node capacitance.

An issue with using TG is that the trigger should be synchronised, so that both PMOS and NMOS turn on and turn off at the same time. Therefore, there needs to be a delay associated with that. On comparing the use of TG with a normal gate driver cell, the delay came to be exactly the same, and did not improve the overall circuit delay from the previous case.

3.3.3 Increasing comparator gain

The next design change attempted was to increase the comparator gain directly by increasing the device sizes in order to be able to drive the power NMOS directly. This will drive up the power consumption of the comparator significantly, but will be able to decrease the overall circuit delay since the gate driver cells will be bypassed.

Before making any changes to the comparator sizing, the output and delay is as shown in Fig. 3.14. It can be noted that there is significant delay, and the node is not able to charge all the way up to 2V before being discharged.

After changing the sizes of the comparator, the output and delay of the comparator is shown in Fig. 3.15. On increasing the comparator gain, the node is able to get charged to 2V, but there is still significant turn-on delay. The turn-off delay seems to be eliminated in this condition.

The main issue with using a comparator with larger gain is the power consump-

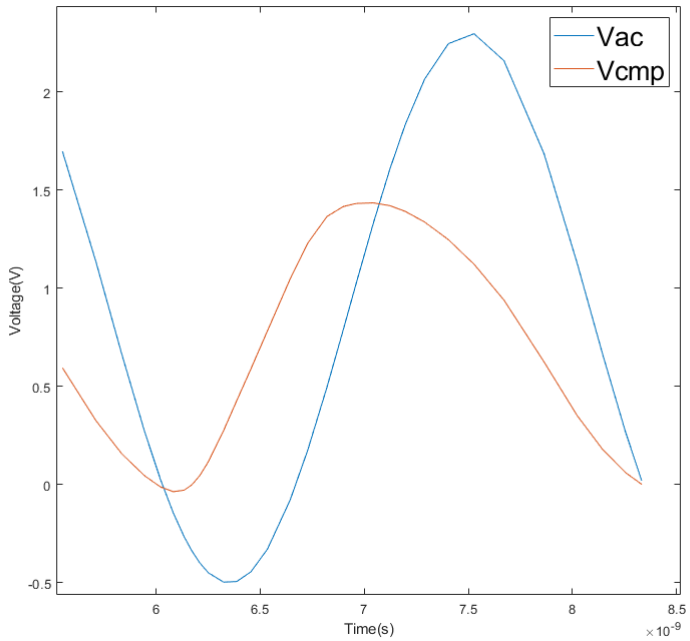


Figure 3.14: Comparator gain and delay before changing sizing

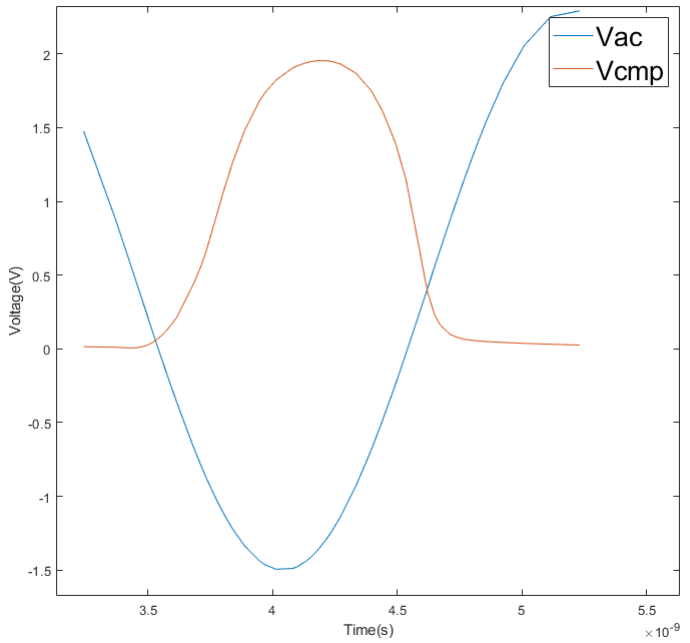


Figure 3.15: Comparator gain and delay after changing sizing

tion. The comparator consumes 2.26mW of power. The AR designed is only capable of harvesting 9mW of power. Furthermore, the comparator is still not able to achieve ZVS, and has a turn-on delay of 0.2ns. The turn off-delay has been eliminated.

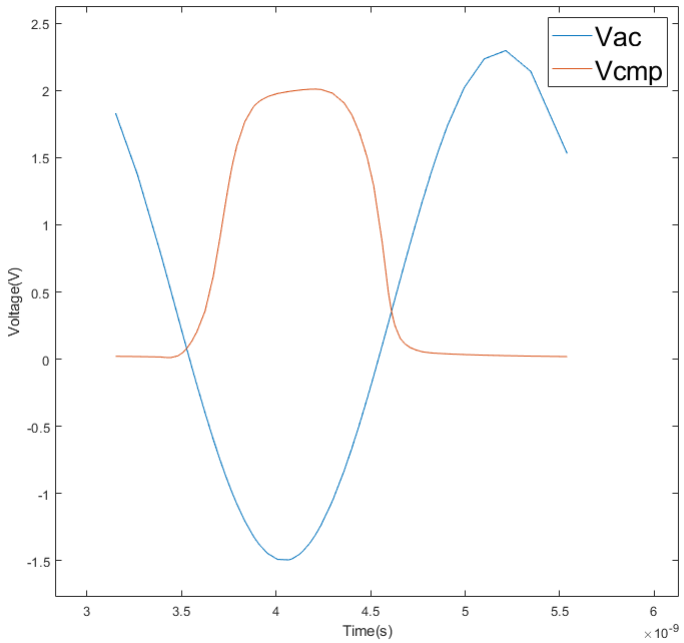


Figure 3.16: Cascaded Rectifier, Comparator driving one stage

3.3.4 Cascading the rectifier stages

It is clear that the large power NMOS size which adds a large capacitive node is the point creating significant delay in the circuit. Another design change attempted was to split the rectifier into three stages and cascade them together, with each stage being 1/3rd the size of the previous rectifier with one stage.

Then, the comparator can be used to drive only one stage, and evaluate for any gains in PCE.

In the testbench, when driving a lower sized NMOS, the output of the comparator is shown in Fig. 3.16. It can be seen that the node charges up quicker than the previous case as expected. The next step would be to evaluate the comparator in a system to find

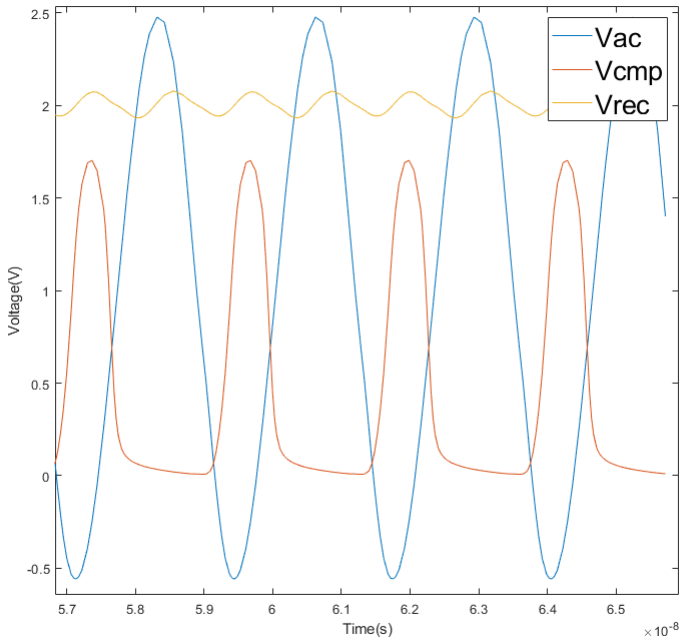


Figure 3.17: Cascaded AR in a system

out the PCE and VCR. The output of that case is shown in Fig. 3.17.

The comparator consumes 1.2mW of power. The turn-on delay is about 0.192ns, When simulating with the system, the output power of the rectifier is 7mW for a load of 500ohm and 2V output voltage. The input power is 13mW. The PCE of the system is 47.7%. There is a significant decrease in PCE compared to the base case. Therefore, it is not a viable option.

3.3.5 System Simulation

Since the design changes made to the comparator to improve the PCE of the rectifier failed. The base cross-coupled rectifier was used in a system to evaluate its working. The system comprises of a cross-coupled rectifier, and a pre-designed Bandgap Reference, and a pre-designed Low-Dropout Regulator which is used to power up the load circuits.

The BGR is used to provide a stable reference voltage to the circuit which is independent of temperature changes. The reason an LDO is used is to regulate the output

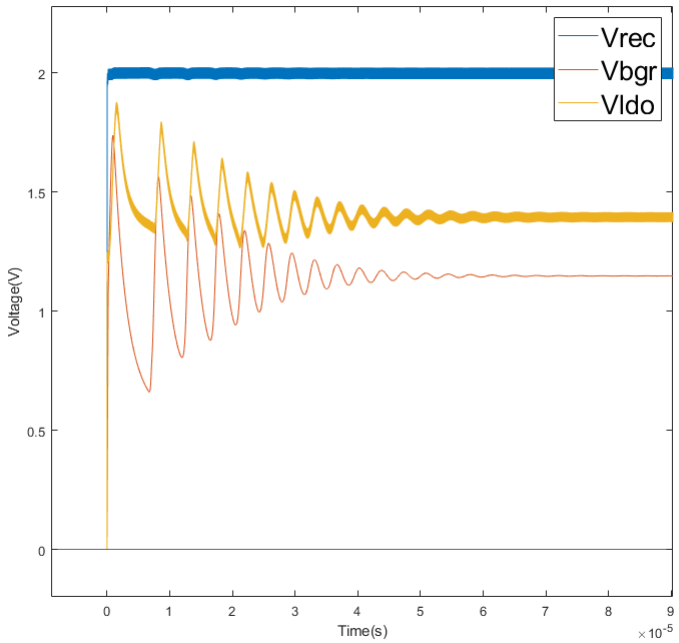


Figure 3.18: System Simulation

voltage as required by the load, and to ensure the output voltage is constant even if the supply voltage or load current is not fixed.

Fig. 3.18 shows the system simulation graphs. The input sinusoidal voltage amplitude is 3V at a system frequency of 433MHz. The input voltage peak seen by the rectifier is 2.52V and the output DC voltage is 2V. Using the Equation. 3.2, the VCR is calculated to be 79.45%.

Using Equation. 3.1, the power consumption of the system can be calculated. The input power is 13.7mW, the output power is 8.07mW, and the calculated PCE is 58.86%

Chapter 4

Conclusion

This thesis report started with a brief literature review on the need for Wireless Power Transfer. It then talks about the on-chip rectifiers and active rectifiers and the issues and compensation techniques that are present to increase the PCE and VCR of the Active Rectifier.

In Chapter 3, the initial section uses the techniques discussed in Chapter 2 to understand the concepts using a pre-designed Active Rectifier for 13.56MHz. At 13.56MHz, the time period and conduction time is fairly large, and does not require high power comparators to operate the power NMOS devices. The delays are also smaller, and within the tolerable range to be compensated for.

Using Voltage Mode compensation, the turn-on and turn-off delay were controlled. The design involved using resistors and switching the offset modes from on-delay elimination to off-delay elimination or vice-versa. An issue with multiple pulsing was encountered when switching occurs. A simple change proposed was to ensure that the offset voltage added to eliminate the on-delay was removed before the offset voltage for the off-delay could be added as well as the other way round. This seems to work for lower frequencies, but will struggle to work as expected when the conduction time is lower.

The second section of Chapter 3 involved using the design from the first section, and making some design changes for it to operate at a higher frequency of 433MHz. The changes made to the design was not able to achieve zero voltage switching.

In the first design, the gate driver cells were using up significant power to drive the power NMOS of the rectifiers and were also adding large delay to the circuit. The VM compensation added to the circuit was not capable of eliminating the delays due to the compensation range of VM is relatively small.

The second design attempted to bypass the gate driver cells with transmission gates. The issue with transmission gates is that they need to be triggered at the same instant, and this causes a delay in the circuit which is comparable to the first design.

The third design attempted to bypass the gate driver cells by increasing the gain of the comparator. This reduces the circuit delay significantly, but also drives up the power consumption of the comparator to make it infeasible to be used to drive the power NMOS.

The fourth design change was to split the rectifier into three stages, and use a comparator to drive the power NMOS of one stage, which was one-third smaller than the previous design with only one stage. This design was then simulated in a circuit, but failed to improve the PCE as compared to the base design.

Since the design changes failed to work successfully, the system simulations were done with a normal cross-coupled rectifier, with a BGR and LDO. The rectifier achieved a PCE of 58.86% and a VCR of 79.45%. The output voltage of the rectifier is 2V.

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Appendix A

System Schematics

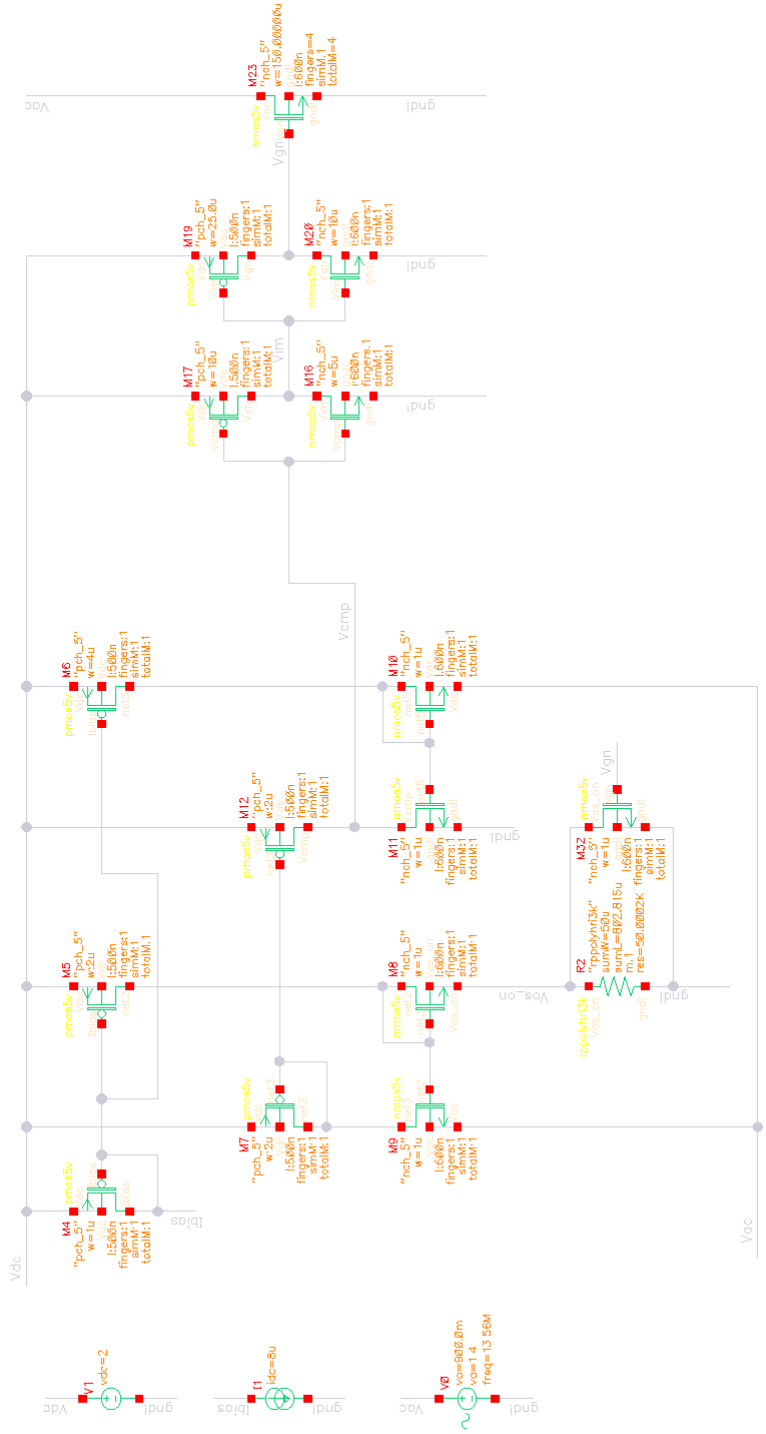

Figure A.1: VM On Delay Elimination - Testbench

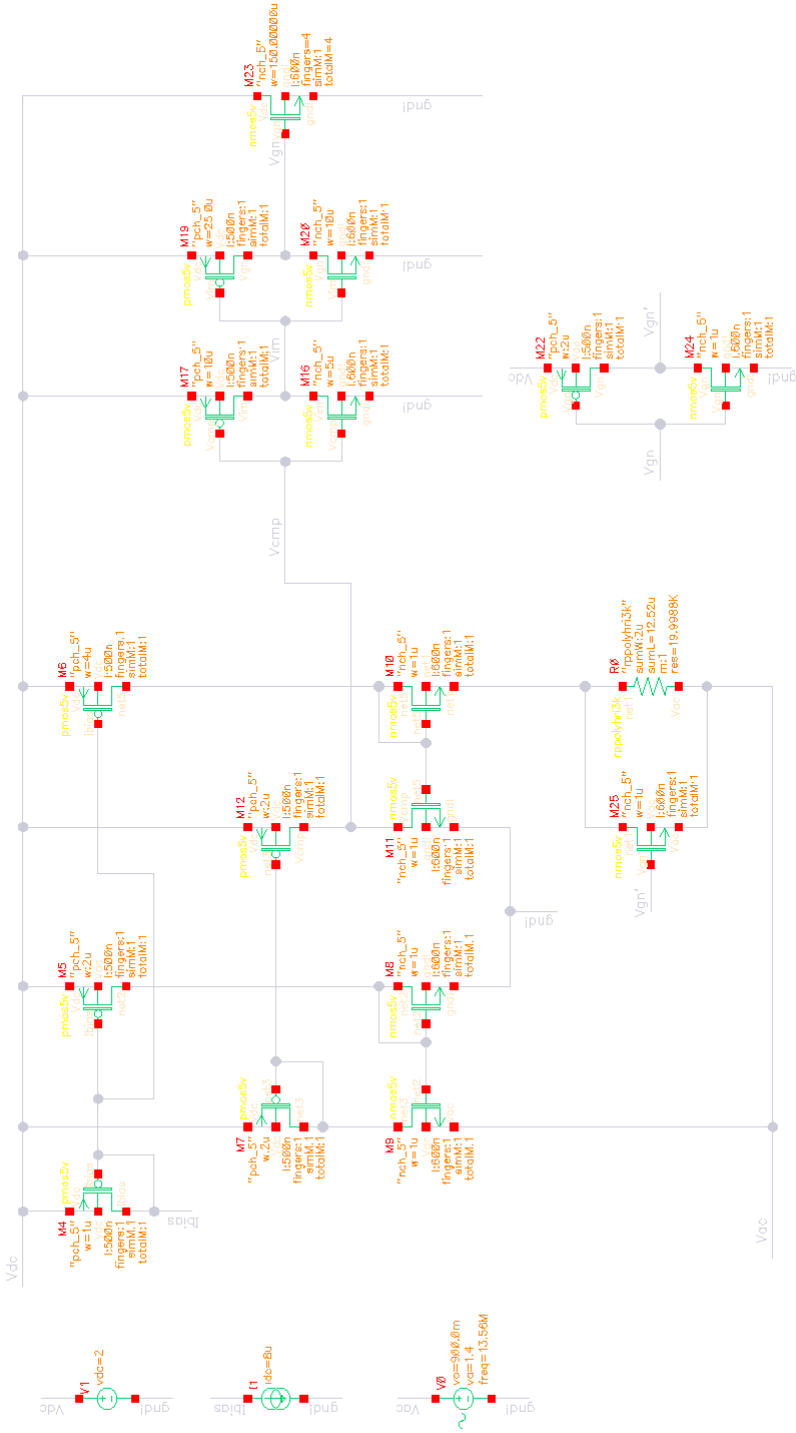

Figure A.2: VM Off Delay Elimination - Testbench

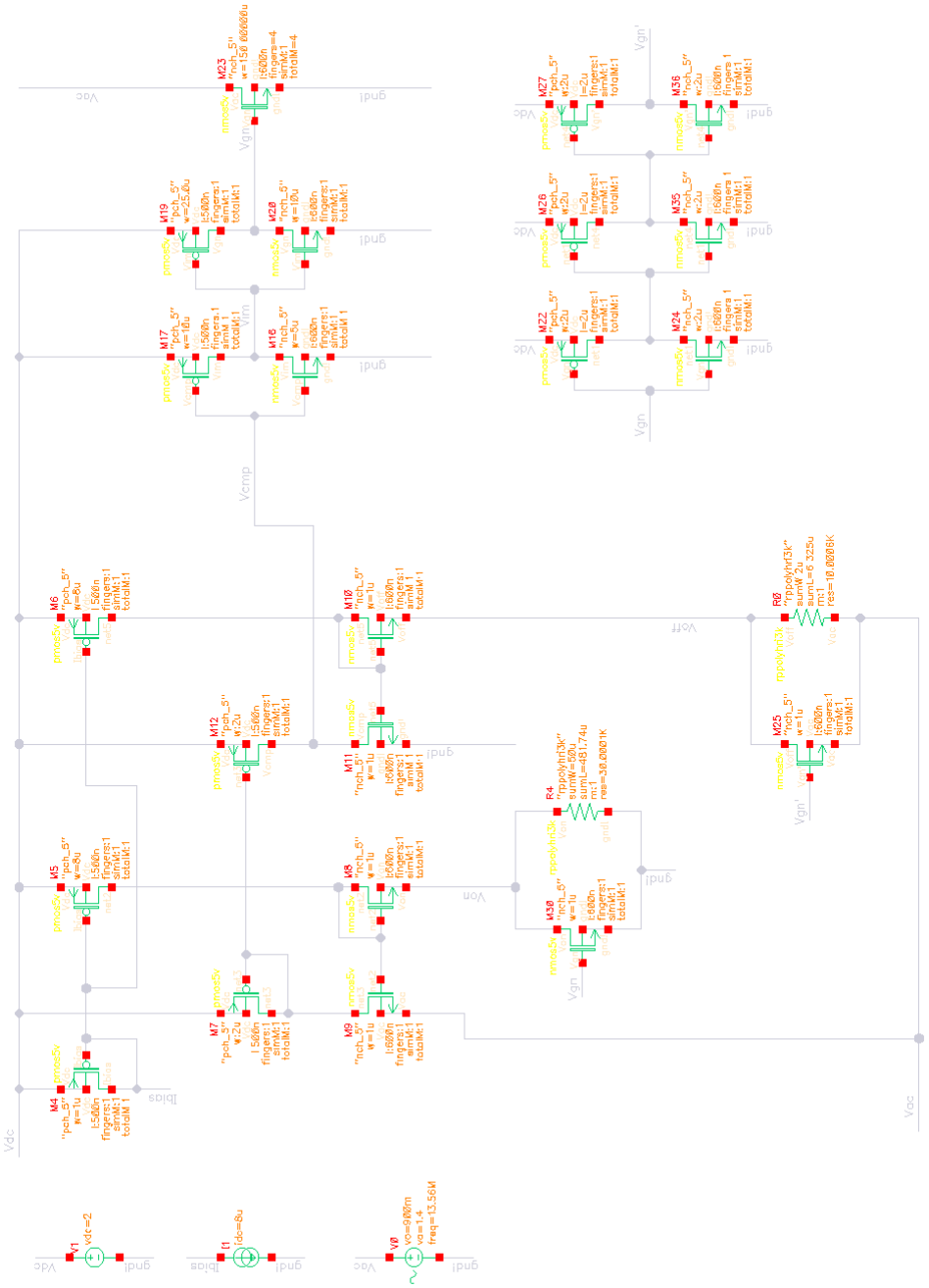

Figure A.3: VM On/Off Delay Elimination - Testbench

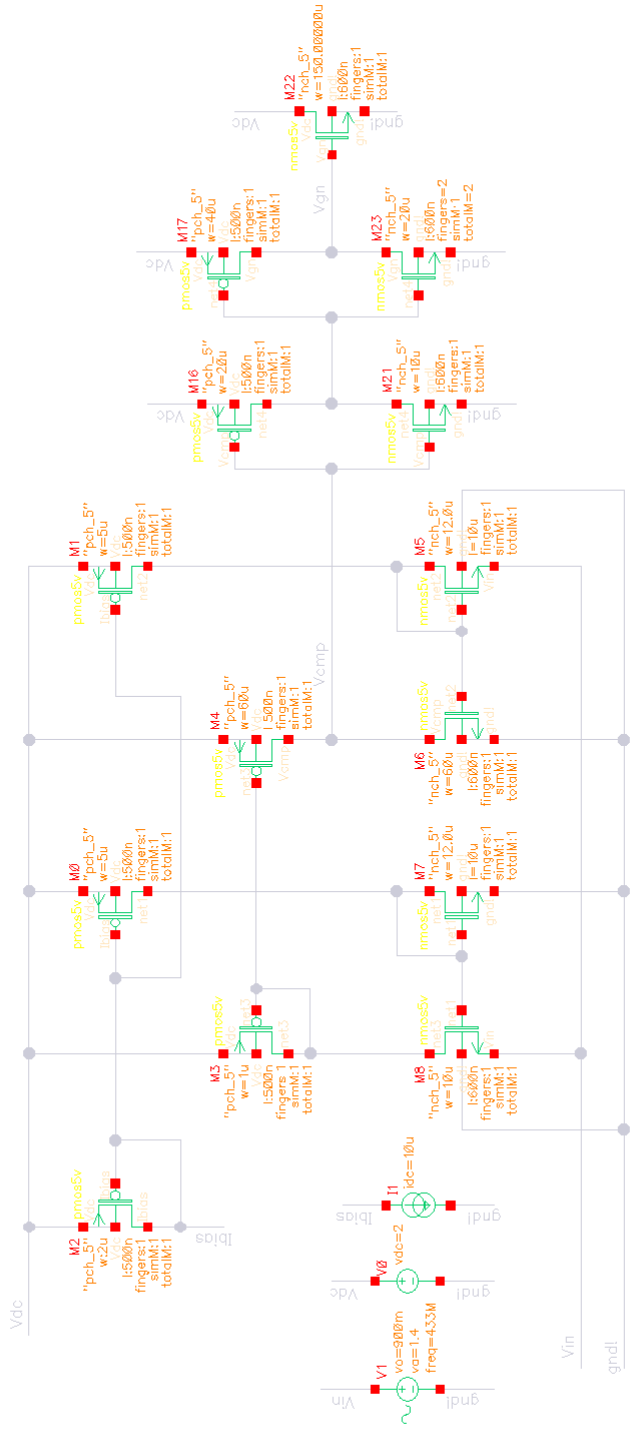

Figure A.4: 443MHz VM - Testbench

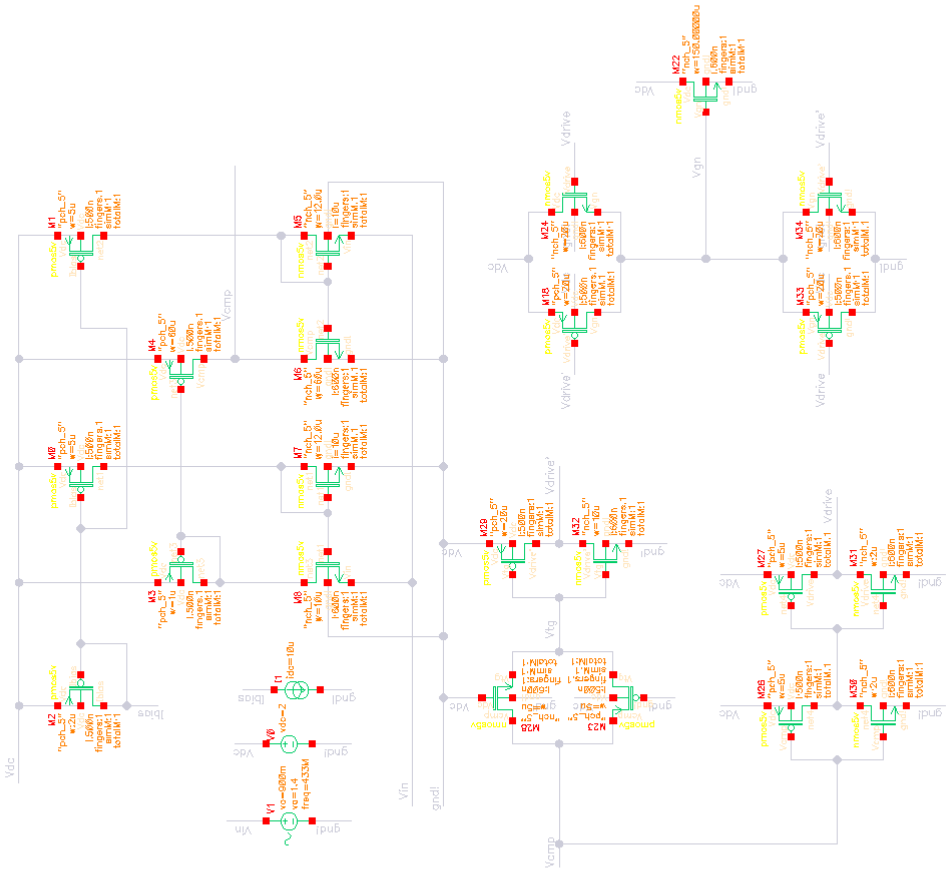

Figure A.5: 443MHz VM and transmission gates - Testbench

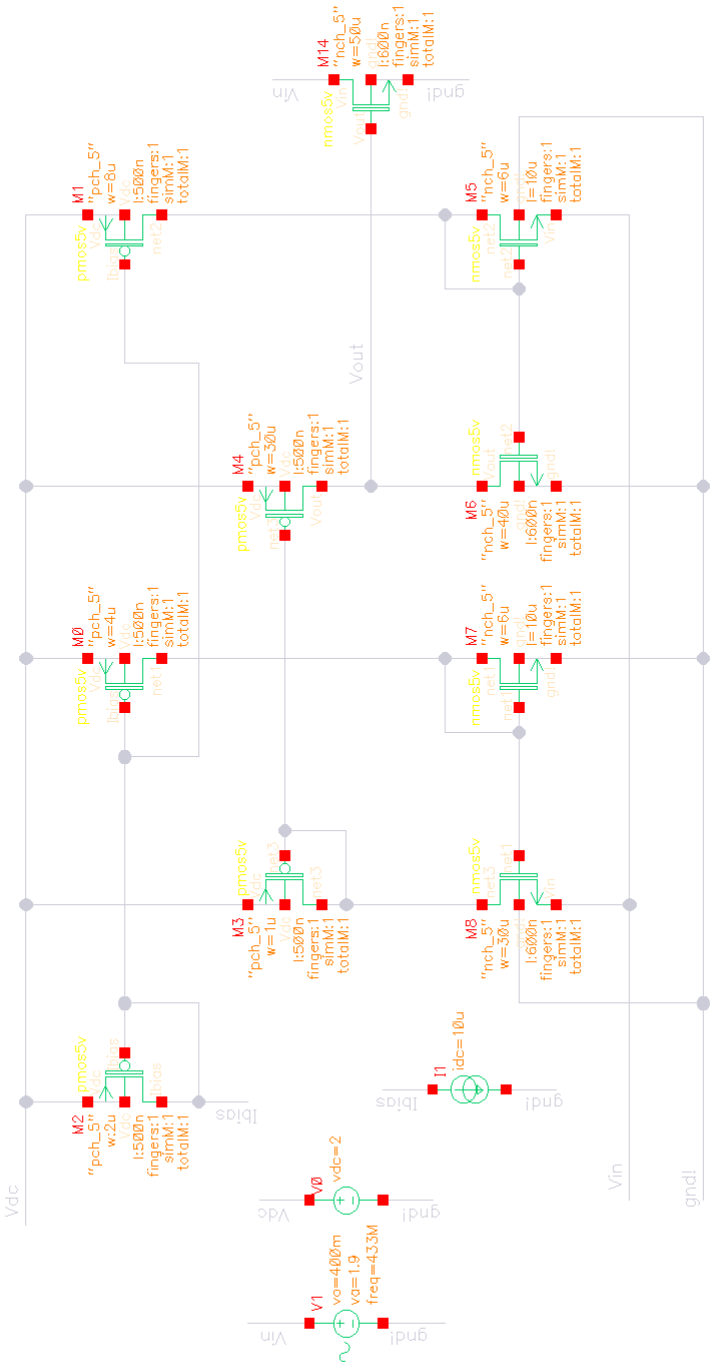

Figure A.6: 443MHz Increasing comparator gain - Testbench

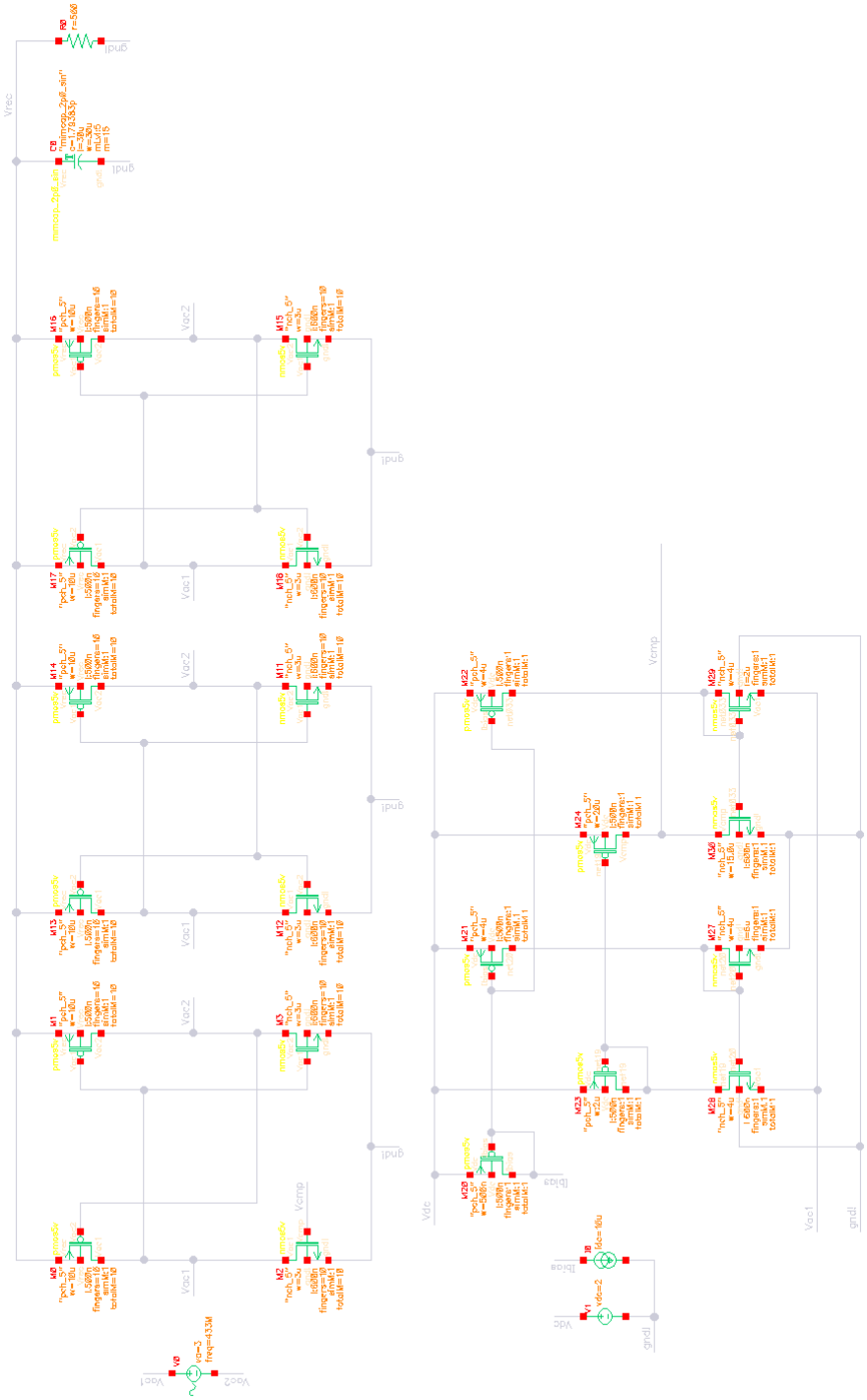

Figure A.7: 443MHz Cascade AR 3 stages - Testbench

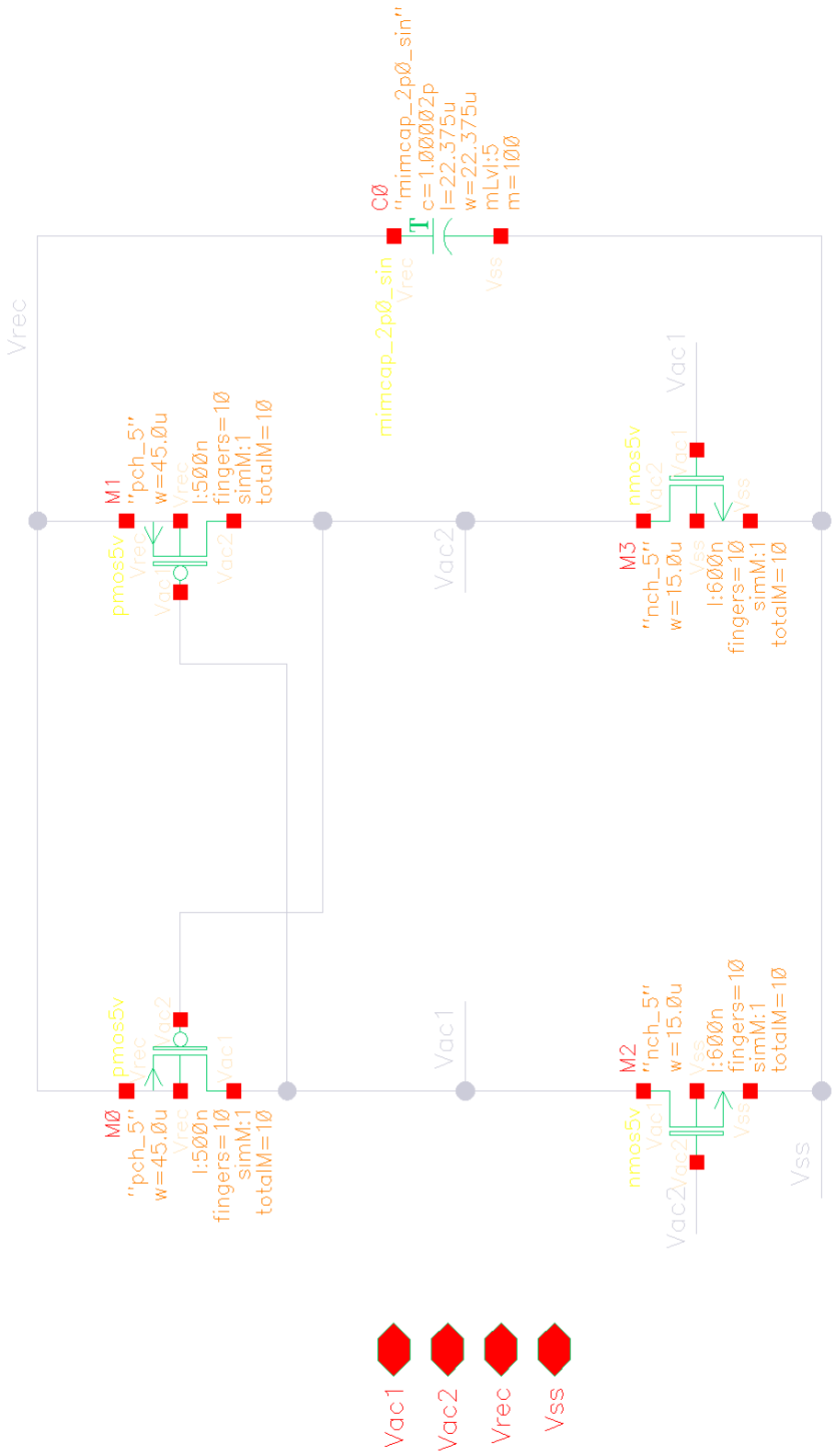

Figure A.8: 443MHz CC Rectifier - Testbench

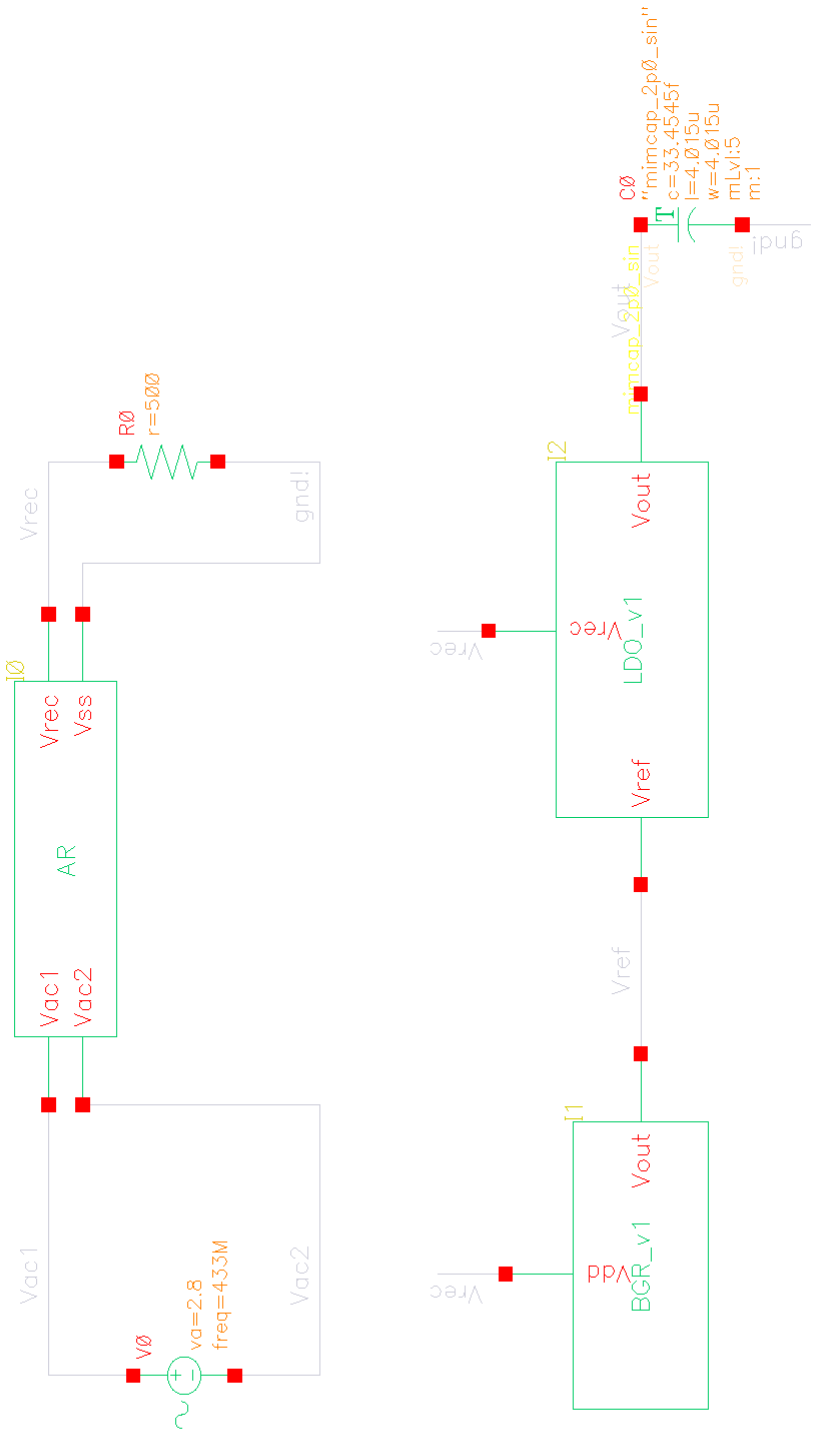

Figure A.9: 443MHz Rectifier System LDO and BGR - Testbench

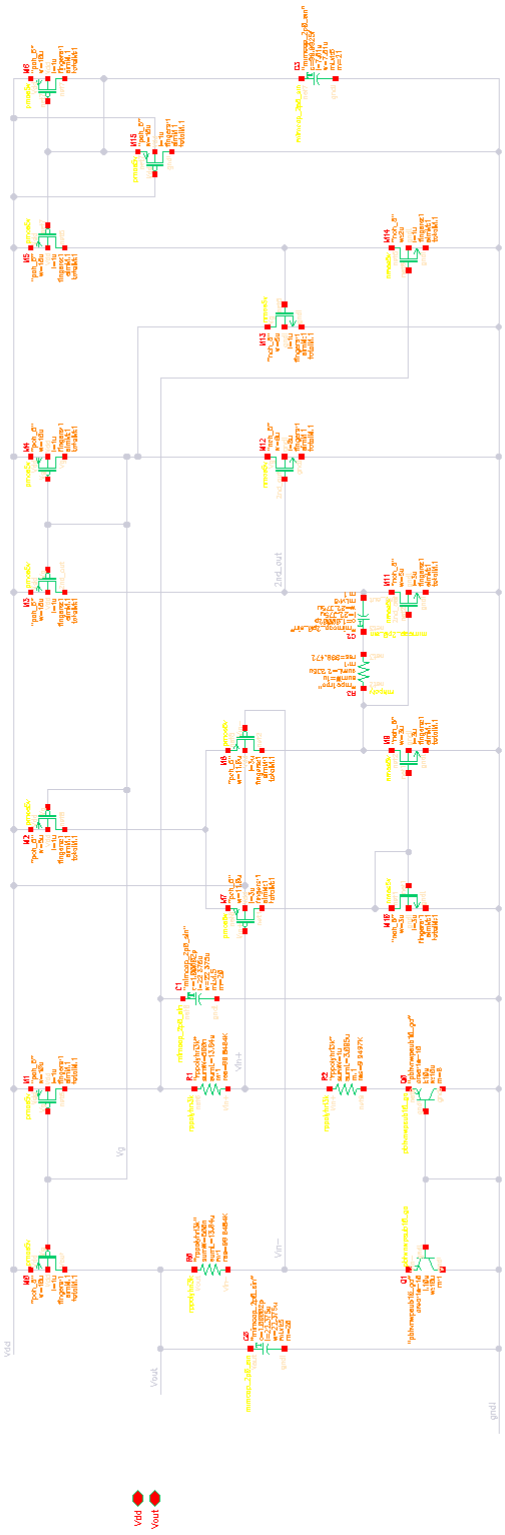

Figure A.10: BGR

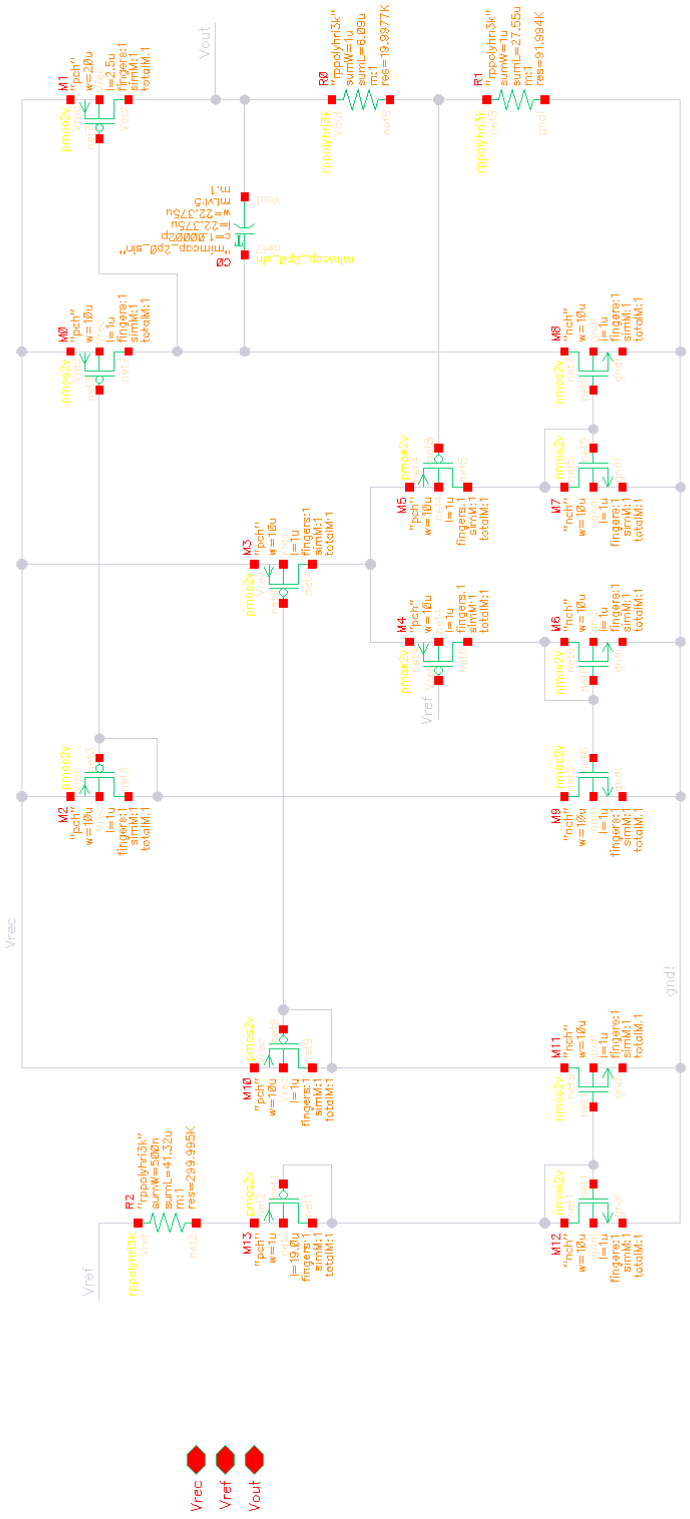

Figure A.11: LDO